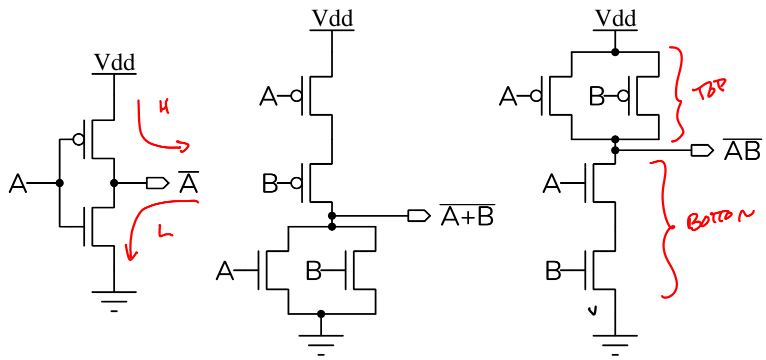
Implementation of Digital Logic Circuits

Exercise 1:



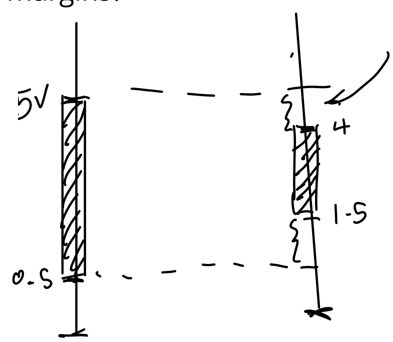
NAND

A	B	TOP	BOTTOM	O/P
0	0	ON	OFF	HIGH
0	1	ON	OFF	
1	0	ON	OFF	
1	1	OFF	ON	LOW

In which direction does the output current flow when the output is high? When it is low? Which transistors in the NAND circuit are on (conducting) in each case?

Exercise 2: A logic family has V_{OH}(min) = 5 V, V_{OL}(max) = 0.5 V, V_{IH}(min) = 4 V and V_{IL}(max) = 1.5 V. What are the noise margins?

- noise margin(low) = $V_{IL(max)} - V_{OL(max)}$
- noise margin(high) = $V_{OH(min)} - V_{IH(min)}$



=Voh - Vih = 5 - 4 = 1V

=Vil - Vol = 1.5 - 0.5 = 1V

Exercise 3: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

$$\frac{P_2}{P_1} = \frac{f_2}{f_1} \cdot \left(\frac{V_2}{V_1}\right)^2$$

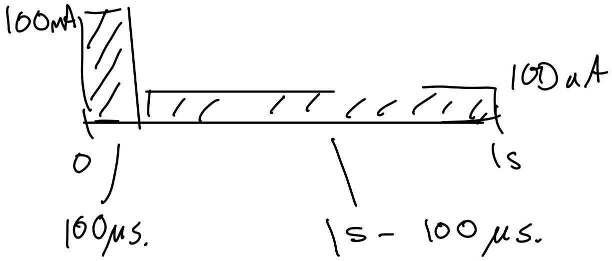
power after change: $P_2 = P_1 \cdot \frac{f_2}{f_1} \cdot \left(\frac{V_2}{V_1}\right)^2$

percent reduction in power consumption: $R = -\frac{(P_2 - P_1)}{P_1} \cdot 100$

percent eduction in power at 3.3 V $R\left(V_1 = 5\,[V], V_2 = 3.3\,[V], f_2 = f_1\right) = \;\; 56$

percent eduction in power at 1 MHz: $R\left(f_1 = 50\,[MHz], f_2 = 1\,[MHz], V_2 = V_1\right) = \;\; 98$

Exercise 4: If a circuit draws $100\,\mathrm{mA}$ for $100\,\mu\mathrm{s}$ per second and draws $100\,\mu\mathrm{A}$ the rest of the time, how long will a $1000\,\mathrm{mAh}$ battery last?



on time, on current: $T_{on} = 100\,[us]\,, I_{on} = 100\,[mA]$

off time, off current: $T_{off} = 1\,[s] - T_{on}, I_{off} = 100\,[uA]$

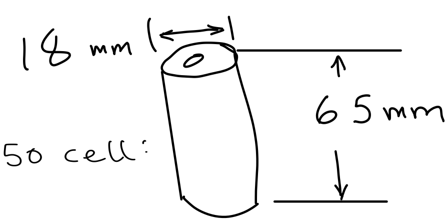
average current: $I_{avg} = \dfrac{I_{on} \cdot T_{on} + \ I_{off} \cdot T_{off}}{T_{on} + T_{off}} = [uA] \quad = 110\,[uA]$

battery capacity: $C = 1000\,[mA \cdot h]$

battery duration: $T = \dfrac{C}{I_{avg}} = [years] \quad = 1.04\,[years]$

Exercise 5: 18650 cells weigh about 50 g, output 3.7 V and have a capacity of 3500 mA-h. How many cells are needed to build an 85 kWh EV battery? How much does it weigh?

18650 cell:



batttery capacity in Joules: $C_{bat} = 85\,[kWh] = \ \ 3.06 \times 10^{8}\,[J]$

$C = \underline{mA} \cdot \underline{h}$

cell capacity in Joules: $C_{cell} = 3.7\,[V] \cdot 3500\,[mA \cdot h] = \ \ 46620\,[J]$

$\frac{P}{V} = I$

number of cells required to make up battery: $N_{cell} = \dfrac{C_{bat}}{C_{cell}} = \ \ 6564$

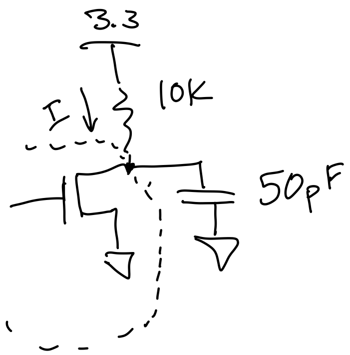
$= \dfrac{85\,kWh}{3.7\,V}$ ≡kVAh

weight of cell: $W_{cell} = 50\,[g] = [g] \quad = 50\,[g]$

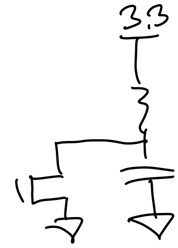
weight of battery: $W_{battery} = W_{cell} \cdot N_{cell} = \ \ 328.2\,[kg]$

$= \dfrac{23\ kA \cdot h}{3.5\ AH}$

Exercise 6: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?



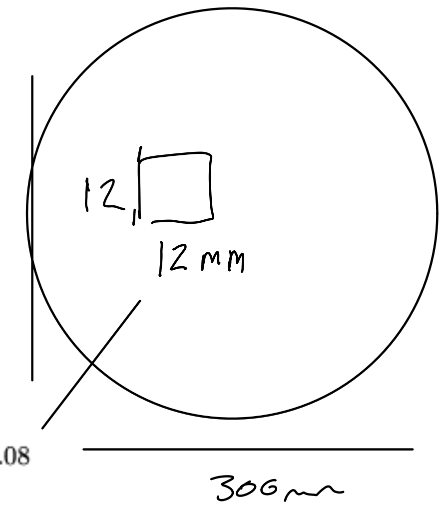
$I = \frac{V}{R} = \underline{\underline{0.33\ mA}}$



$\tau = RC = 10\times10^{3}\cdot 50\times10^{-12}$

$= 500\times10^{-9} = \underline{\underline{0.5\mu s.}}$

Exercise 7: The Apple M3 CPU has an area of approximately $146\,\mathrm{mm}^2$. How many die fit on one 300 mm wafer? If each wafer costs $20,000 to manufacture, what is the cost per die?



die per wafer: $N = \frac{\pi\cdot\left(\frac{300\,[mm]}{2}\right)^2}{146\,[mm^2]} = 484.15$

$\sqrt{146} = 12.08$

cost per die: $\frac{20000}{N} = 41.31$

Exercise 8: How many square mm of PCB area does each package require? Which packages have their pins accessible when the package is placed on the PCB?

TQFP: area $= 22\ mm^2 \approx 2000\ mm^2$

BGA area $= 3.5\ mm^2 \approx 12\ mm^2$