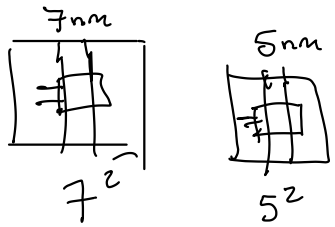
Implementation Technologies

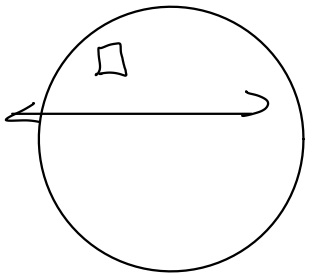
Exercise 1: What improvement in number of transistors per unit area would be achieved by reducing the feature size from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?



area with 5nm feature $= 5 \times 5$

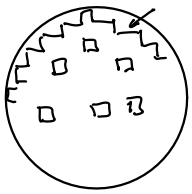
" " 7nm " $= 7 \times 7$

area ratio $= \frac{5}{7^2} = \frac{25}{49} \approx \frac{1}{2}$



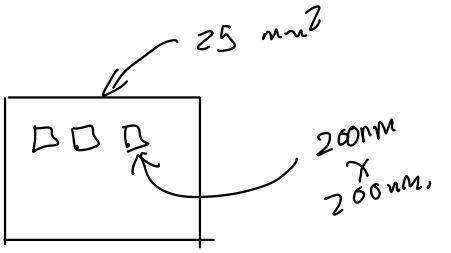
area of circle $= \pi r^2 = \pi \left(\frac{300}{2}\right)^2$

$\approx 70{,}000\ mm^2$



$\#\text{die} = \frac{70{,}000}{(5 \times 5)} = 3{,}000$

$\#\text{gates} = \frac{\text{area of die}}{\text{area of gate}} = \frac{(5 \times 5) \times (10^{-3})^2\ m^2}{(0.2 \times 0.2) \times (10^{-6})^2\ m^2} = \frac{25 \times 10}{.04} = 625 \times 10^6$ gates



200 nm = 0.2 μm

$= 0.2 \times 10^{-6}$

Exercise 2: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

1 month TTM: PLD

100×10^6 volume: ASIC

unclear reqmts: PLD

high perf CPU: ASIC.