

Implementation Technologies

Exercise 1: What improvement in number of transistors per unit area would be achieved by reducing the feature size from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?

Exercise 2: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?