Timers and Clock Dividers

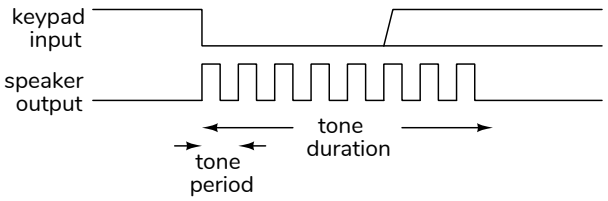
You may not submit a video demonstration for this lab. You must demonstrate your solution in person during your scheduled lab session. The lab instructor will then ask you to make changes to demonstrate that you understand your design. You are unlikely to complete this lab unless you start with a working solution.

Version 2: Added more details to frequency measurement instructions and example screen capture.

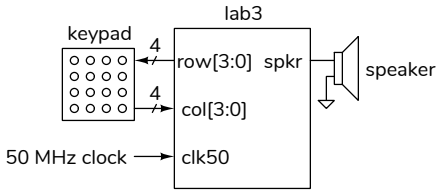
Introduction

Counters can be used to create delays (timers) and periodic signals (clock dividers).

In this lab you will design a circuit that uses one counter as a clock divider to generate a waveform of a specific frequency and another counter as a timer to set the duration of the waveform. You will use this signal to drive a speaker which will result in an audible tone.



You will connect the keypad as in previous labs and connect a speaker to a CPLD pin:



Your counters will use the 50 MHz clock on the CPLD board. The period of this clock is $T = 1/50\times10^6 = 20$ ns.

Components

You will need:

- your CPLD board, Byte Blaster JTAG interface and mini-USB power connector,
- the matrix keypad
- the speaker from your ELEX 2117 parts kit
- jumper cables with alligator clips from your ELEX 1117 parts kit[1])
- a USB flash drive to store the 'scope waveform

Requirements

The last three digits of your BCIT ID (n_1, n_2, and n_3) determine the key that starts the tone, the tone duration and its frequency.

For example, if your BCIT ID is . A00123$\boxed{4}\boxed{5}\boxed{6}$ then $n_1 = \boxed{4}$, $n_2 = \boxed{5}$ and $n_3 = \boxed{6}$.

Design your circuit so that:

1. keypad key $\boxed{n_1}$ starts the tone,
2. the frequency of the tone is $f = 500 + n_2 \times 100$ Hz,
3. the tone lasts for $1 + n_3/3$ seconds.

For example, for an ID ending in 456, pressing keypad $\boxed{4}$ should generate a $500 + \boxed{5} \times 100 = 1000$ Hz tone for $1 + \boxed{6}/3 = 3$ seconds.

The tone should last for the required duration even if the key is released before the end of the tone duration.

Hints

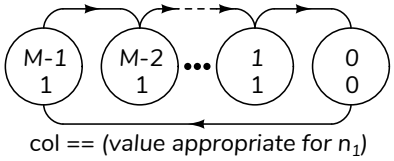
Your solution will use two counters: one to determine the tone duration and another to generate the tone frequency.

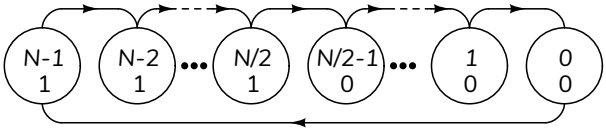
A simple implementation for the timer is a down-counter that is set to $M - 1$ when the appropriate key is pressed and stops when it reaches zero. The tone is output whenever the counter is not zero. The duration of the timer will be MT where T is the clock period.

[1] You can put alligator clips over the banana plugs.

A simple implementation for the clock divider is a down-counter that is set to $N-1$ whenever it reaches zero.

State transition diagrams for these counters are be:





If the speaker output is set high only when the timer's counter value is non-zero *and* the clock divider's counter value is greater than $N/2$ then the speaker output will be a square wave of the appropriate duration and frequency.

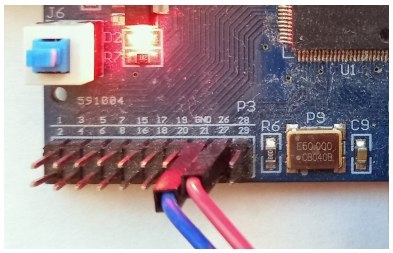
There are other possible solutions. For example, the clock divider could have a period of half of the tone period and toggle (invert) the output when the count reaches zero. This requires a 1-bit (**spkr**) register.

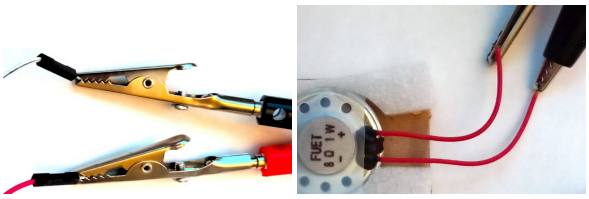
Another option is for the timer to count cycles of the clock divider output instead of cycles of the 50 MHz clock.

CPLD I/O

The following diagram shows the connections to the CPLD:

Connect the matrix keypad to the CPLD as in previous labs. Connect a CPLD I/O pin to the speaker pin and a ground pin with alligator clip cables (pin 26 was used as the **spkr** pin here, a ground pin is next to it):





Pre-Lab

Have the following ready to show at the start of your lab:

(a) The values of n_1, n_2, and n_3 corresponding to your BCIT ID.

(b) The corresponding button to be pushed, tone frequency and duration.

(c) The value of **col** when $\boxed{n_1}$ is pressed.

(d) The values of N and M (defined above) for your values of n_2, and n_3.

(e) A block diagram of your solution. Follow the instructions in the report and video guidelines document.

Procedure

Create a project, compile it, and configure the CPLD.

If you use the same keypad pins as in the previous lab and Pin 26 for the speaker output, you should end up with the following pin assignments:

To	Assignment Name	Value
row[3]	Location	PIN_99
row[2]	Location	PIN_97
row[1]	Location	PIN_95
row[0]	Location	PIN_91
col[3]	Location	PIN_89
col[2]	Location	PIN_87
col[1]	Location	PIN_85
col[0]	Location	PIN_83
clk50	Location	PIN_12
spkr	Location	PIN_26
led	Location	PIN_77
col	Weak Pull-Up Resistor	On

You can import these pin assignments above from the **lab3.qsf** file on the course website.

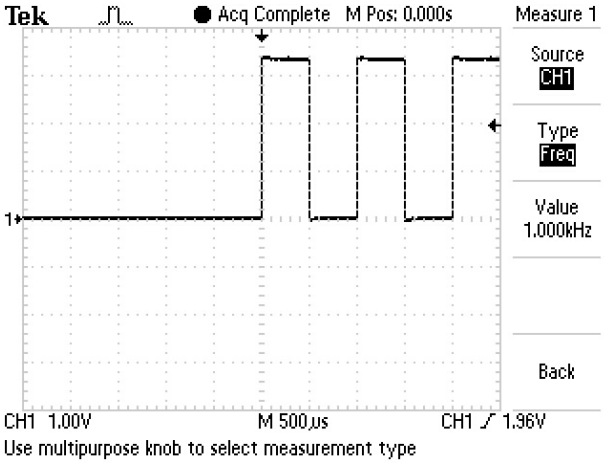
For troubleshooting you can assign internal signals to the **led** output on pin 77 . A high level turns on this on-board LED.

Test your design by listening for a tone of the appropriate duration and measuring the frequency with the oscilloscope.

Oscilloscope Measurements

Manuals for the Tektronix TDS 1012 oscilloscope are available on the course website.

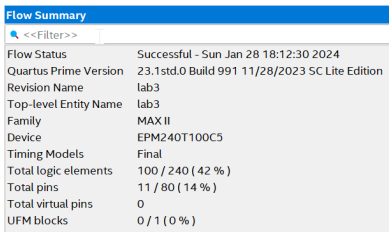
Measure the signal's frequency as follows: connect the probe and its ground clip to the appropriate jumper pins; set the probe to 10X if necessary; press DEFAULT SETUP (twice if necessary); adjust the vertical scale (Vertical CH 1 Volts/Div knob) to 1 V per division; set the horizontal scale (Horizontal Sec/Div knob) to about half the period of your waveform; set the trigger level (Trigger Level knob) to about 2 V; enable frequency measurement (press MEASURE, select the top button Ch 1, then select Freq for Type); press SINGLE SEQ (to capture a single waveform); press the appropriate keypad key to generate a tone (this should capture one waveform and the trigger status will change from Ready to Acq. Complete); verify the measured frequency is correct; save the display to a USB drive (plug in the USB drive, press PRINT, wait until the clock icon disappears and a message shows the operation is complete; the **.JPG** image file may be in a sub-directory named **ALL**).



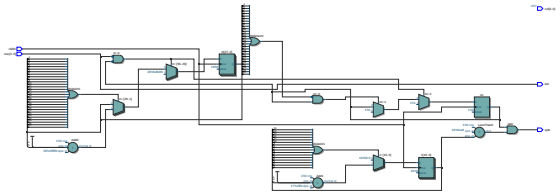
Demonstration and Submission

To get credit for completing this lab you must demonstrate it to the lab instructor during your assigned lab session *and* submit a PDF document containing the following to the appropriate Assignment folder on the course website:

1. The answers to the Pre-Lab questions.
2. A listing of your Verilog code.
3. A screen capture of your compilation report (**Window** > **Compilation Report**) similar to:



4. The schematic created by **Tools > Netlist Viewers > RTL Viewer** and then **File > Export...**. For example:



5. A screen capture of the 'scope measurement of the **spkr** waveform, including the frequency measurement.