Practice Lab

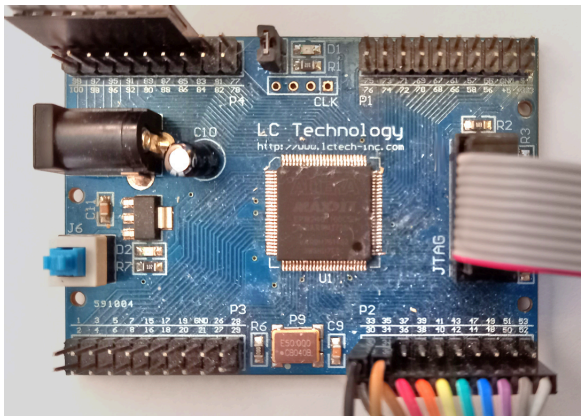
Version 2: Changed "FPGA" to "CPLD".

Introduction

In this lab you will learn about the CPLD board, logic synthesis with Quartus, writing lab reports and creating video demonstrations. You are strongly encouraged to submit a lab report and video for marking although the mark will not count towards your final lab mark.

Intel MAX II CPLD Board

This board contains an Altera EPM240T100C5 MAX II complex programmable logic device (CPLD). A CPLD is an IC that can be programmed to implement different logic functions. This board will be used for most labs. The board's schematic is available on the course website.



The CPLD has 100 pins. The board has four 20-pin headers that allow you to connect to most of the CPLD pins. CPLD pin numbers are marked next to each header pin. You will use these pins to connect components such as an LED display and a keypad.

The CPLD's I/O pins use 3.3V logic levels. To avoid damaging the board, *never connect your circuits to an external power supply or use the on-board 5V supply*.

The board also has an active-high LED connected to CPLD pin 77 and a 50 MHz clock oscillator connected to CPLD pin 12. We will use these on-board components for this lab.

The board is powered through a coaxial power connector which must be connected to a USB port or USB power supply. *The USB-Blaster cannot power the board (even though it lights the power LED).*

The board is programmed through the JTAG connector which must be connected to the USB-Blaster from your ELEX 1117 parts kit.

Quartus Prime and ModelSim

Quartus is a logic synthesizer – software that converts a hardware description language (HDL) description of your circuit to a file that can program the CPLD over the JTAG port. We will use the System Verilog HDL in this course.

Pre-Lab

Read these notes and bring your CPLD board and USB Blaster to the lab.

Procedure

Install the Software

Follow the instructions in the Software Installation and Use document to install Quartus, ModelSim, and MAX II device support. Install the USB-Blaster driver dated 2009-04-21 (version 2.4.16.0) from the course web site.

You can also use Quartus from AppsAnywhere although this requires a network connection when using the software.

Logic Synthesis

Create a project named **lab0** and add a System Verilog file named **lab0.sv** containing the following code:

```
// lab0.sv
// ELEX 2117 practice lab - LED blinker
// your name, date

module lab0 (
        input logic clk,
        output logic led ) ;

        logic [25:0] count ;
        always_ff @(posedge clk)
                count <= count + 1'b1 ;

        assign led = count[25] ;

endmodule
```

Follow the logic synthesis instructions to synthesize **lab0.sv**. Assign the **led** signal to pin 77 and the **clk** signal to pin 12. Program the CPLD. The jumper labelled J2 (next to LED) must be installed.

If everything went right, the on-board LED will start blinking.

Lab Report

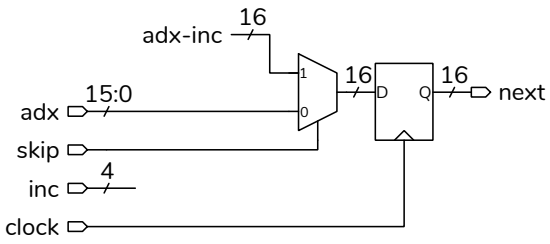
Follow the Report and Video Guidelines document to create a lab report that includes the following:

- a listing of your **lab0.sv** file formatted as explained in the Report and Video Guidelines document. Use your own name and the correct date.

- a screen capture of the compilation report for **lab0** (**Window > Compilation Report**) similar to:

ow Status	Successful - Wed Jan 4 23:26:27 2023
Quartus Prime Version	22.1std.0 Build 915 10/25/2022 SC Lite Edition
Revision Name	lab0
Top-level Entity Name	lab0
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	23 / 240 (10 %)
Total pins	2 / 80 (3 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

- a copy of the following block diagram (redraw it, don't copy-and-paste)



Submissions

Submit the following to the appropriate assignment folders on the course web site: (a) a report containing the items described above, and (b) a short video of your CPLD board showing the LED blinking. Orient the video so that the LED is at the top of the video.