ELEX 2117 : Digital Techniques 2
2025 Winter Term

FINAL EXAM
2:30 PM – 5:30 PM
Wednesday, April 17, 2025
SW01-1205

This exam has nine (9) questions on eight (8) pages. The marks for each question are as indicated. There are a total of forty-five (45) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 11 marks

A state machine controls a door that opens for 6 seconds when a button is pushed. A **`button`** input is asserted when the button is pushed. **`open`** and **`close`** outputs control a motor. The **`closed`** and **`opened`** inputs are asserted when the door is closed or opened respectively. The **`clk`** clock input frequency is 100 Hz. The Verilog module implementing this state machine is declared:

```
module controller ( input logic clk, button, opened, closed, output logic open, close ) ;
```

Neither output should be asserted until **`button`** is asserted. Then **`open`** should be asserted until **`opened`** is asserted. Then there should be a 6 second delay with neither output asserted. Then **`close`** should be asserted until **`closed`** is asserted. Then the state machine should wait for the next push of **`button`**.

Write a **`controller`** module to implement this state machine. You may assume the controller starts in a valid state. Declare any additional signals required. Follow the course coding conventions but do not include comments. *Hints: Start by deciding on the states, their encodings, and the outputs in each state. You can implement the delay with a counter that is decremented in the state where the door is open and is initialized to its maximum value in other states.*

Question 2 — 4 marks

A logic circuit consumes 20 mW with a clock frequency of 1 MHz and a voltage of 5 V. What clock frequency would allow this circuit to operate for one year (8760 hours) from a 2 V, 200 mA-hour battery?

Question 3 — 6 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hA6` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h6`
`x[1] & x`	
`x + 2 >> 1`	
`x >> 1 * 2`	
`x > {y,y} ^ x != x`	
`x[3] ? y[0] : y`	
`x[1] ? 2 ? 3 : 4 : 5`	

Question 4 — 8 marks

Write a System Verilog testbench named **`mult_tb`** to test a **`mult`** module declared as:

```
module mult (
   input logic [31:0] a, b,
   output logic [31:0] c,
   input logic clk, valid,
   output logic ready ) ;
```

Your testbench must instantiate the module and supply it with a 10 MHz clock on **`clk`**.

The testbench must do the following, in order: set **`a`** to **`32'd11`** and **`b`** to **`32'd2`**, assert **`valid`**, wait until **`ready`** is asserted, print the string **`"error"`** if the value of **`c`** is not equal to **`32'd22`**, and terminate the simulation.

Declare all signals used in your testbench. Do not write or declare the **`mult`** module. Do **not** do anything else in your testbench such as reading or writing files (including **`.vcd`** files). Omit comments.

Question 5 — 2 marks

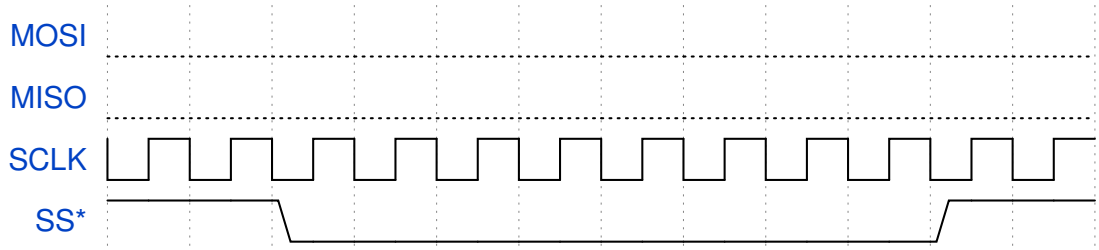
A logic family has $V_{IH}(\min) = 0.7$ V and $V_{IL}(\max) = 0.4$ V. What $V_{OH}(\min)$ and $V_{OL}(\max)$ levels would result in a noise margin of 0.2 V for both high and low logic levels?

Question 6 — 2 marks

What is the maximum clock frequency that would result in reliable operation for a circuit whose maximum delay through any combinational logic path is 30 ns and that uses registers with a clock-to-output delay of 2 ns and a minimum setup time requirement of 6 ns?

Question 7 — 3 marks

The diagram below shows the waveforms of an SPI interface that follows the conventions described in the lecture notes. Fill in *one* of the two missing waveforms so that the 8-bit value 8'h27 is transferred from the **master to the slave**. *Note: No marks will be awarded if you fill in both waveforms.*



Question 8 — 4 marks

You wish to sample the signal from a sensor so that it can be analyzed on a computer. The signal contains frequency components up to 50 kHz. You would like the quantization noise power to be less than 0.1% of the signal power. You can assume that the equation for the quantization SNR of a sine wave applies to this signal.

(a) What sampling rate(s) should you use?

(b) What is the minimum number of bits of ADC resolution that should be used?

Question 9 — 5 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term.

Moore's Law	
ASIC	
FPGA	
fabless	
wafer	
die	
NRE	
SoC	
LE	
LUT	

(1) programmable logic with 1000's of flip-flops

(2) often a few square mm in area

(3) most semiconductor companies

(4) historical rate of increase

(5) LUT plus a flip-flop

(6) a memory storing output values

(7) ASIC plus CPU

(8) product development costs

(9) 300mm diameter

(10) made for a specific application

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This exam paper is for:

Sample Exam 2 A01234567

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Question 1 — 11 marks

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Write a **`controller`** module to implement this state machine. You may assume the controller starts in a valid state. Declare any additional signals required. Follow the course coding conventions but do not include comments. *Hints: Start by deciding on the states, their encodings, and the outputs in each state. You can implement the delay with a counter that is decremented in the state where the door is open and is initialized to its maximum value in other states.*

Question 2 — 4 marks

A logic circuit consumes 10 mW with a clock frequency of 1 MHz and a voltage of 5 V. What clock frequency would allow this circuit to operate for one year (8760 hours) from a 2 V, 200 mA-hour battery?

Question 3 — 6 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h38` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h8`
`x[1] & x`	
`x + 2 >> 1`	
`x >> 1 * 2`	
`x > {y,y} ^ x != x`	
`x[3] ? y[0] : y`	
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What is the maximum clock frequency that would result in reliable operation for a circuit whose maximum delay through any combinational logic path is 50 ns and that uses registers with a clock-to-output delay of 2 ns and a minimum setup time requirement of 10 ns?

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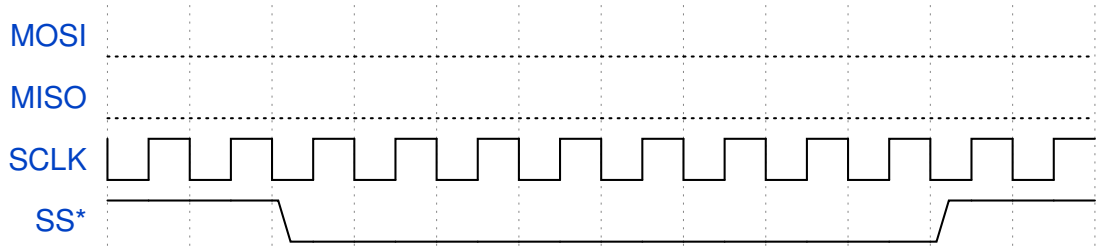
The diagram below shows the waveforms of an SPI interface that follows the conventions described in the lecture notes. Fill in *one* of the two missing waveforms so that the 8-bit value 8'h1b is transferred from the **slave to the master**. *Note: No marks will be awarded if you fill in both waveforms.*



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