Solutions to Quiz 5

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

What is the maximum propagation delay through any combinational logic path for a digital circuit operating with a 33 (or 40) MHz clock and registers that require setup times of more than 3 ns and have a clock-to-output delay of less than 2 ns?

Answers

For a clock frequency of 33 MHz the clock period is ≈ 30 ns, and for a clock frequency of 40 MHz the clock period is 25 ns.

The equation for the available setup time is:

$$t_{SU}\,(\text{avail}) = T_{clock} - t_{CO}\,(\text{max}) - t_{PD}\,(\text{max})$$

from which the maximum propagation delay is:

$$t_{PD}\,(\text{max}) = T_{clock} - t_{CO}\,(\text{max}) - t_{SU}\,(\text{avail})$$

By setting t_{CO} and t_{SU} to their minimum values we find the maximum allowed propagation delay:

$$t_{PD}(\text{max}) = 30\ (\text{or } 25) - 3 - 2 = \boxed{25\,\text{ns (or } 20\,\text{ns)}}$$

Question 2

A circuit consumes 1 W at a supply voltage of 5 (or 3.3) V. All else being equal, what supply voltage would reduce the power consumption to 100 mW?

Answers

The ratio of the power consumption at two different frequencies and voltages is:

$$\frac{P_2}{P_1} = \frac{f_2}{f_1} \cdot \left(\frac{V_2}{V_1}\right)^2$$

In this question the ratio P_2/P_1 is 100 mV/1 V = 0.1. Since the frequency is unchanged then $f_2/f_1 = 1$ and we can solve for V_2 as:

$$V_2 = V_1\sqrt{\frac{P_2}{P_1}} = 5\ (\text{or } 3.3) \cdot \sqrt{0.1} \approx \boxed{1.6\,\text{V (or } 1.0\,\text{V)}}$$