ELEX 2117 : Digital Techniques 2
2024 Winter Term

Quiz 5
11:30 AM – 12:20 (no later) PM
Tuesday, March 19, 2024
SW01-1025

This exam has two (2) questions on two (2) pages. The marks for each question are as indicated. There are a total of six (6) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 3 marks

What is the maximum propagation delay through any combinational logic path for a digital circuit operating with a 40 MHz clock and registers that require setup times of more than 3 ns and have a clock-to-output delay of less than 2 ns?

Question 2 — 3 marks

A circuit consumes 1 W at a supply voltage of 3.3 V. All else being equal, what supply voltage would reduce the power consumption to 100 mW?

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Paper, Test 2 A00123456

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Question 1 — 3 marks

What is the maximum propagation delay through any combinational logic path for a digital circuit operating with a 33 MHz clock and registers that require setup times of more than 3 ns and have a clock-to-output delay of less than 2 ns?

Question 2 — 3 marks

A circuit consumes 1 W at a supply voltage of 5 V. All else being equal, what supply voltage would reduce the power consumption to 100 mW?