

ELEX 2117 : Digital Techniques 2
2024 Winter Term

Quiz 4

11:30 AM – 12:20 (or 1:20) PM

Tuesday, February 27, 2024

SW01-1021

This exam has two (2) questions on two (2) pages. The marks for each question are as indicated. There are a total of fourteen (14) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1

8 marks

Fill in the testbench module at right with code that uses **initial** and **always** statements, not loops, to do the following:

```
module quiz_tb ;
  logic [7:0] n ;
```

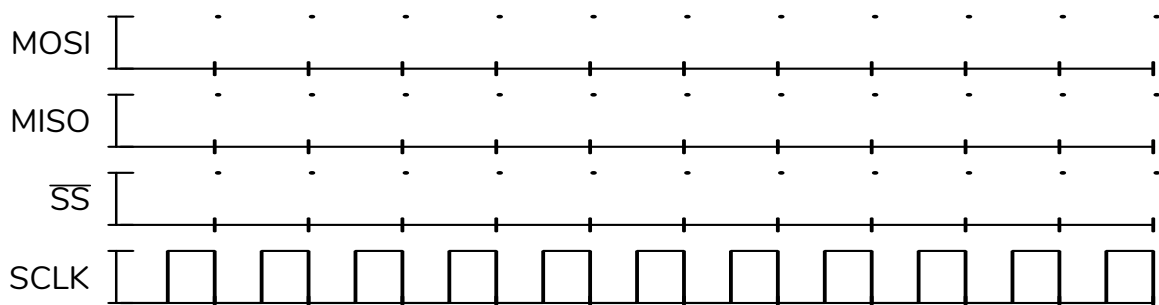
- (a) set the initial value of **n** to 0
- (b) terminate the simulation with **\$stop()** if the value of **n** is ever greater than **8'd127**,
- (c) add 2 to **n** every $10\mu\text{s}$, and
- (d) print the current value of **n** every $40\mu\text{s}$ (using **\$display()**)

```
endmodule
```

Question 2

6 marks

Draw the $\overline{\text{SS}}$, **MISO**, and **MOSI** waveforms that would be used to transfer bytes with values **8'h63** (in Verilog notation) from the slave to the master and **8'h72** from the master to the slave over an SPI interface. Follow the conventions shown in the lecture notes, including the timing of $\overline{\text{SS}}$ relative to the data, the data relative to **SCLK**, and the bit order.



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Question 1

8 marks

Fill in the testbench module at right with code that uses **initial** and **always** statements, not loops, to do the following:

```
module quiz_tb ;
  logic [7:0] n ;
```

- (a) set the initial value of **n** to 0
- (b) terminate the simulation with **\$stop()** if the value of **n** is ever equal to **8'd127**,
- (c) add 1 to **n** every $5\mu\text{s}$, and
- (d) print the current value of **n** every $20\mu\text{s}$ (using **\$display()**)

```
endmodule
```

Question 2

6 marks

Draw the $\overline{\text{SS}}$, **MISO**, and **MOSI** waveforms that would be used to transfer bytes with values **8'h36** (in Verilog notation) from the slave to the master and **8'h27** from the master to the slave over an SPI interface. Follow the conventions shown in the lecture notes, including the timing of $\overline{\text{SS}}$ relative to the data, the data relative to **SCLK**, and the bit order.

