Solutions to Quiz 3

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] y ;
logic [3:0] x ;
```

and that `y` has the value `8'h3a` (or `8'hc9`) and that `x` has the value `4'h6` (or `4'h5`). The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`y[3:0]`	`4'ha (or 4'h9)`
`{!y, ~x}`	
`x >> y[7] ? 0 : 4`	
`^(y[3:0] ^ y[7:4])`	

Answers

For `y = 8'h3a` and `x = 4'h6`:

expression	value
`y[3:0]`	`4'ha`
`{!y, ~x}`	`5'h9`
`x >> y[7] ? 0 : 4`	`32'h0`
`^(y[3:0] ^ y[7:4])`	`1'h0`

and for `y = 8'hc9` and `x = 4'h5`:

expression	value
`y[3:0]`	`4'h9`
`{!y, ~x}`	`5'ha`
`x >> y[7] ? 0 : 4`	`32'h0`
`^(y[3:0] ^ y[7:4])`	`1'h0`

Question 2

A timer uses a counter that counts down from 29,999 (or 59,999) to zero.

(a) What clock frequency would result in a timer duration of 1 ms?

(b) What minimum register width is required to implement this counter? Give your answer in bits.

Answers

(a) The duration, 1×10^{-3} seconds is NT where N is the number of clock cycles and T is the clock period. The clock frequency is $f = \frac{1}{T}$ so we can solve $1 \times 10^{-3} = \frac{N}{f}$ for $f = \frac{N}{1\times10^{-3}} = \frac{30000}{1\times10^{-3}} =$ $\boxed{30\,\text{MHz}}$ (or $\frac{60000}{1\times10^{-3}} = \boxed{60\,\text{MHz}}$.

(b) An n-bit counter an count from 0 to $2^n - 1$ where n is the number of bits. We can solve for the value of n that results in a maximum count value greater than or equal to the count values above: $2^n - 1 \geq 29999$, or $n \geq \log_2(30000) = 14.9$ so a $\boxed{\text{15-bit}}$ (or $\boxed{\text{16-bit}}$) counter is needed.

Question 3

Write a Verilog module named **`vcount`** with a clock input named **`clk`**, a one-bit input named **`fast`** (or **`slow`**), and a one-bit output named **`out`**. Within the module define a 16-bit array named **`count`**. The value of **`count`** should be updated on each clock edge as described below. You do not need to initialize the value of **`count`**. Set the value of **`out`** to the most significant bit of **`count`**. Follow the course coding guidelines but omit comments.

count	fast	next count
0	x	16'hffff
n	0	$n-1$
n	1	$n-3$

or:

count	slow	next count
0	x	16'hf000
n	0	$n-4$
n	1	$n-2$

Answers

```
module vcount
  ( input logic clk, fast,
    output logic out ) ;

   logic [15:0] count ;

   always_ff @(posedge clk)
     count <= !count ? 16'hffff :
              !fast ? count-1 : count-3 ;

   assign out = count[15] ;

endmodule

// or:

module vcount_
  ( input logic clk, slow,
    output logic out ) ;

   logic [15:0] count ;

   always_ff @(posedge clk)
     count <= !count ? 16'hf000 :
              !slow ? count-4 : count-2 ;

   assign out = count[15] ;

endmodule
```

For which Quartus generates the following schematics: