**ELEX 2117 : Digital Techniques 2**
**2024 Winter Term**

**Quiz 3**
**11:30 AM – 12:20 (or 1:20) PM**
**Tuesday, February 13, 2024**
**SW01-1021**

This exam has three (3) questions on two (2) pages. The marks for each question are as indicated. There are a total of ten (10) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

# Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____



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## Question 1 — 3 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] y ;
logic [3:0] x ;
```

and that `y` has the value `8'hc9` and that `x` has the value `4'h5`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

| expression | value |
|---|---|
| `y[3:0]` | `4'h9` |
| `{!y, ~x}` | |
| `x >> y[7] ? 0 : 4` | |
| `^(y[3:0] ^ y[7:4])` | |

## Question 2 — 2 marks

A timer uses a counter that counts down from 59,999 to zero.

(a) What clock frequency would result in a timer duration of 1 ms? Show your work. Give your answer in MHz. Show units.

(b) What minimum register width is required to implement this counter? Give your answer in bits. Give your answer in bit. Show units.

## Question 3 — 5 marks

Write a Verilog module named **`vcount`** with a clock input named **`clk`**, a one-bit input named **`slow`**, and a one-bit output named **`out`**. Within the module define a 16-bit array named **`count`**. The value of **`count`** should be updated on each clock edge as described below. You do not need to initialize the value of **`count`**. Set the value of **`out`** to the most significant bit of **`count`**. Follow the course coding guidelines but omit comments.

| count | slow | next count |
|---|---|---|
| 0 | x | 16'hf000 |
| $n$ | 0 | $n-4$ |
| $n$ | 1 | $n-2$ |

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# Paper, Test 2 A00123456

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## Question 1 — 3 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] y ;
logic [3:0] x ;
```

and that `y` has the value `8'h3a` and that `x` has the value `4'h6`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

| expression | value |
|---|---|
| `y[3:0]` | `4'ha` |
| `{!y, ~x}` | |
| `x >> y[7] ? 0 : 4` | |
| `^(y[3:0] ^ y[7:4])` | |

## Question 2 — 2 marks

A timer uses a counter that counts down from 29,999 to zero.

(a) What clock frequency would result in a timer duration of 1 ms? Show your work. Give your answer in MHz. Show units.

(b) What minimum register width is required to implement this counter? Give your answer in bits. Give your answer in bit. Show units.

## Question 3 — 5 marks

Write a Verilog module named **`vcount`** with a clock input named **`clk`**, a one-bit input named **`fast`**, and a one-bit output named **`out`**. Within the module define a 16-bit array named **`count`**. The value of **`count`** should be updated on each clock edge as described below. You do not need to initialize the value of **`count`**. Set the value of **`out`** to the most significant bit of **`count`**. Follow the course coding guidelines but omit comments.

| count | fast | next count |
|---|---|---|
| 0 | x | 16'hffff |
| $n$ | 0 | $n-1$ |
| $n$ | 1 | $n-3$ |