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ELEX 2117 : Digital Techniques 2 2024 Winter Term

Quiz 2 11:30 AM – 12:20 (or 1:20) PM Tuesday, January 30, 2024 SW01-1021

This exam has two (2) questions on two (2) pages. The marks for each question are as indicated. There are a total of eleven (11) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. <u>Underline</u> or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work**.

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult. Answer your own exam. Do not start until you are told to do so.

Name: _____

BCIT ID:

Signature:

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ELEX 2117 Quiz 1

A00123456



Question 1

4 marks **Question 2**

7 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

logic [7:0] y ; logic [3:0] x ;

and that **y** has the value **8'h63** and that **x** has the value **4'b1001**. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
y[3:0]	4 ' h3
x + y	
x[2:1] ? y : !y	
~ y[3:2] & 15	
y >> 4 > ~ x	

rough work below

Write one **always_ff** statement and one **assign** statement in the incomplete System Verilog module below so that the module implements the following state transition diagram:



The diagram follows the course conventions: each state bubble shows the value of st(ate) above the value of o in that state; both in binary. Transitions are labelled with expressions involving the inputs. You may assume stis initialized to 2'b00. Follow the course coding guidelines but omit comments.

module q2					
(input logic s, x, c	Locl	κ,			
output logic [1:0] o))	;			
logic [1:0] st ;	11	write	your	code	below

endmodule

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ELEX 2117 Quiz 1

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Question 1

4 marks Question 2



Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

logic [7:0] y ; logic [3:0] x ;

and that **y** has the value **8** ' **h9c** and that **x** has the value **4** ' **b0110**. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
y[3:0]	4 ' hc
x + y	
x[2:1] ? y : !y	
~ y[3:2] & 15	
y >> 4 > ~ x	

rough work below

Write one **always_ff** statement and one **assign** statement in the incomplete System Verilog module below so that the module implements the following state transition diagram:



The diagram follows the course conventions: each state bubble shows the value of st(ate) above the value of **o** in that state; both in binary. Transitions are labelled with expressions involving the inputs. You may assume **st** is initialized to **2** ' **b00**. Follow the course coding guidelines but omit comments.

```
module q2
( input logic s, x, clock,
    output logic [1:0] o );
logic [1:0] st ; // write your code below
```

endmodule