Solutions to Quiz 1

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hc3` (or `8'h59`) and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

Answers

For `x=8'hc3` and `y=4'b0101`:

expression	value
x[3:0]	4'h3
{ y, x[7:4] }	8'h5c
!x[3:2]	1'h1
{~x,!x}	9'h78
x ? 3'b1 : 4'b1	4'h1
x[7] ? 1 : 2	32'h1
y[0] ? x : y	8'hc3

and for `x=8'h59` and `y=4'b0101`:

expression	value
x[3:0]	4'h9
{ y, x[7:4] }	8'h55
!x[3:2]	1'h0
{~x,!x}	9'h14c
x ? 3'b1 : 4'b1	4'h1
x[7] ? 1 : 2	32'h2
y[0] ? x : y	8'h59

Question 2

Write a Verilog literal that has a width of 5 (or 8) bits, uses a binary (or hexadecimal) base and has a value of 2 (or 16) (decimal).

Answers

`5'b10` or `8'h10`.

Question 3

Write a Verilog module named `select` that has one 16-bit logic input named `w`, a logic input named `upper` (or `lower`) and an 8-bit logic output named `x`. The value of `x` should be set to bits 15 down to 8 (or 7 down to 0) of `w` if `upper` (or `lower`) is non-zero, otherwise to bits 7 down to 0 (or 15 down to 8) of `w`. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.

Answers

```
module select
  ( input logic [15:0] w ,
    input logic lower,
    output logic [7:0] x ) ;

   assign x = lower ? w[7:0] : w[15:8] ;

endmodule

module select_
  ( input logic [15:0] w ,
    input logic upper,
    output logic [7:0] x ) ;

   assign x = upper ? w[15:8] : w[7:0] ;

endmodule
```

From which Quartus generates the following schematics: