ELEX 2117 : Digital Techniques 2
2024 Winter Term

Quiz 1
11:30 AM – 12:20 (or 13:20) PM
Tuesday, January 16, 2024
SW01-1021

This exam has three (3) questions on two (2) pages. The marks for each question are as indicated. There are a total of eleven (11) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 6 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h59` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h9`
`{ y, x[7:4] }`	
`!x[3:2]`	
`{~x,!x}`	
`x ? 3'b1 : 4'b1`	
`x[7] ? 1 : 2`	
`y[0] ? x : y`	

Question 2 — 2 marks

Write a Verilog literal that has a width of 8 bits, uses a hexadecimal base and has a value of 16 (decimal).

Question 3 — 3 marks

Write a Verilog module named `select` that has one 16-bit logic input named `w`, a logic input named `lower` and an 8-bit logic output named `x`. The value of `x` should be set to bits 7 down to 0 of `w` if `lower` is non-zero, otherwise to bits 15 down to 8 of `w`. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.

rough work below

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Paper, Test 2 A00123456

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Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 6 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hc3` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h3`
`{ y, x[7:4] }`	
`!x[3:2]`	
`{~x,!x}`	
`x ? 3'b1 : 4'b1`	
`x[7] ? 1 : 2`	
`y[0] ? x : y`	

Question 2 — 2 marks

Write a Verilog literal that has a width of 5 bits, uses a binary base and has a value of 2 (decimal).

Question 3 — 3 marks

Write a Verilog module named `select` that has one 16-bit logic input named `w`, a logic input named `upper` and an 8-bit logic output named `x`. The value of `x` should be set to bits 15 down to 8 of `w` if `upper` is non-zero, otherwise to bits 7 down to 0 of `w`. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.

rough work below