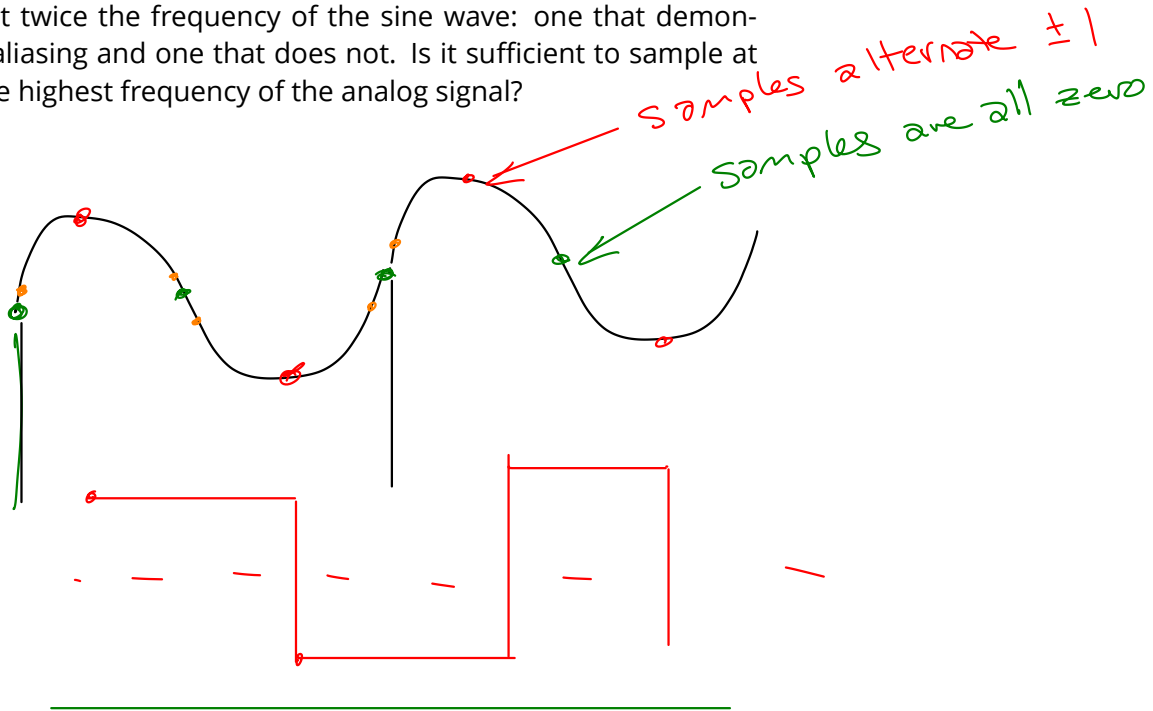


Analog Interfaces

Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one that demonstrates aliasing and one that does not. Is it sufficient to sample at twice the highest frequency of the analog signal?



Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to include frequency components up to the 7th harmonic (at 70 kHz)?

$$\begin{aligned} \text{sample rate} &> 2 \times f_{\max} \\ &> 2 \times 70 \text{ kHz} \\ &> 140 \text{ kHz} \end{aligned}$$

Exercise 3: A signal with range of ± 3 V must be quantized so that the quantization error is less than 1 mV. What minimum number of bits of resolution is required?

$$\begin{aligned} \Delta &= 2 \text{ mV} \\ V &= 3 - (-3) = 6 \text{ V} \\ \text{steps} &= \frac{6}{0.002} = 3000 \\ 2^n - 1 &> 2999 \\ 2^n &> 3000 \\ \log_2 2^n &> \log_2 3000 \\ n &> 11.55 \\ \text{use } n &= 12 \text{ bits} \end{aligned}$$

$\Delta/2$ is worst-case quantization error

Exercise 4: A signal-to-noise power ratio of about 48 dB is considered "good enough" for speech communication. Approximately how many bits per sample are required to obtain this quantization SNR?

$$\frac{S}{N} > 48 \text{ dB}$$

$$1.76 + 6n > 48$$

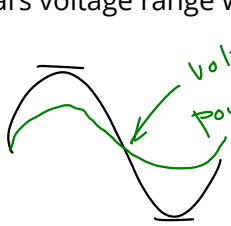
$$6n \gtrsim 46$$

$$n \gtrsim 8$$

Exercise 5: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

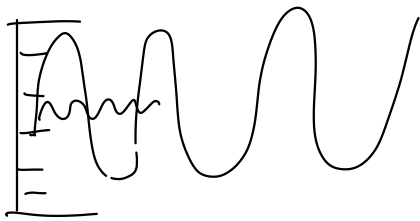
$$10 \log_{10}(2^{2n}) = 6 \text{ dB}$$

$$10 \log_{10}(2) = 3$$



$$\text{SNR} = 1.76 + 6 \cdot 12 = 73.76 \text{ dB}$$

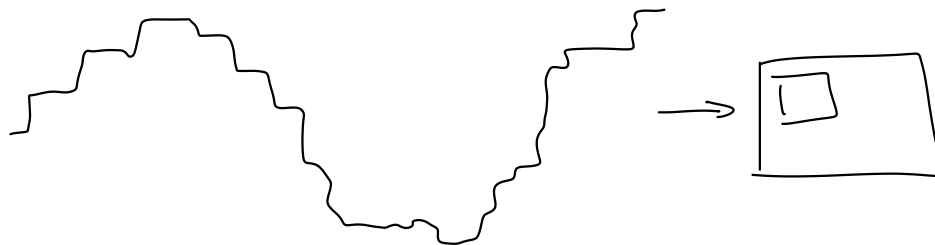
$$\text{SNR} = 73.76 - 6 = 67.76 \text{ dB}$$



OR: only have 11 bits of resolution

$$\text{SNR} = 1.76 + 6 \cdot 11 = 67.6 \text{ dB}$$

Exercise 6: A DAC outputs a digitized 1 kHz sine-wave signal. The analog output is analyzed and the power at 1 kHz is found to be 1 W while the power at all other frequencies adds up to 10 mW. What is the ENOB?



$$S = 1 \text{ W}$$

$$N = 10 \text{ mW}$$

$$\frac{S}{N} = \frac{1}{0.01} = 100$$

$$\frac{S}{N} = 10 \log_{10}(100) = 20 \text{ dB}$$

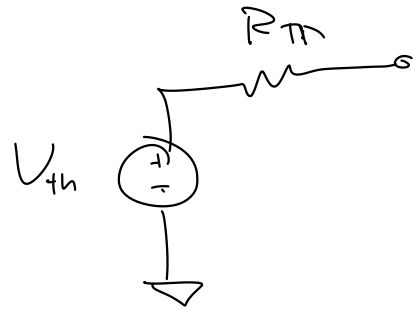
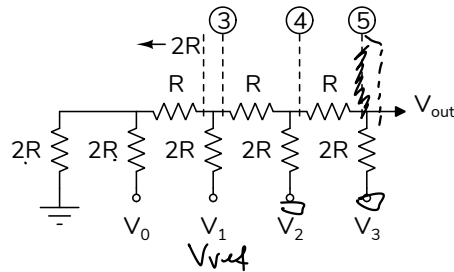
$$20 \text{ dB} = 1.76 + 6n$$

$$18 = 6n$$

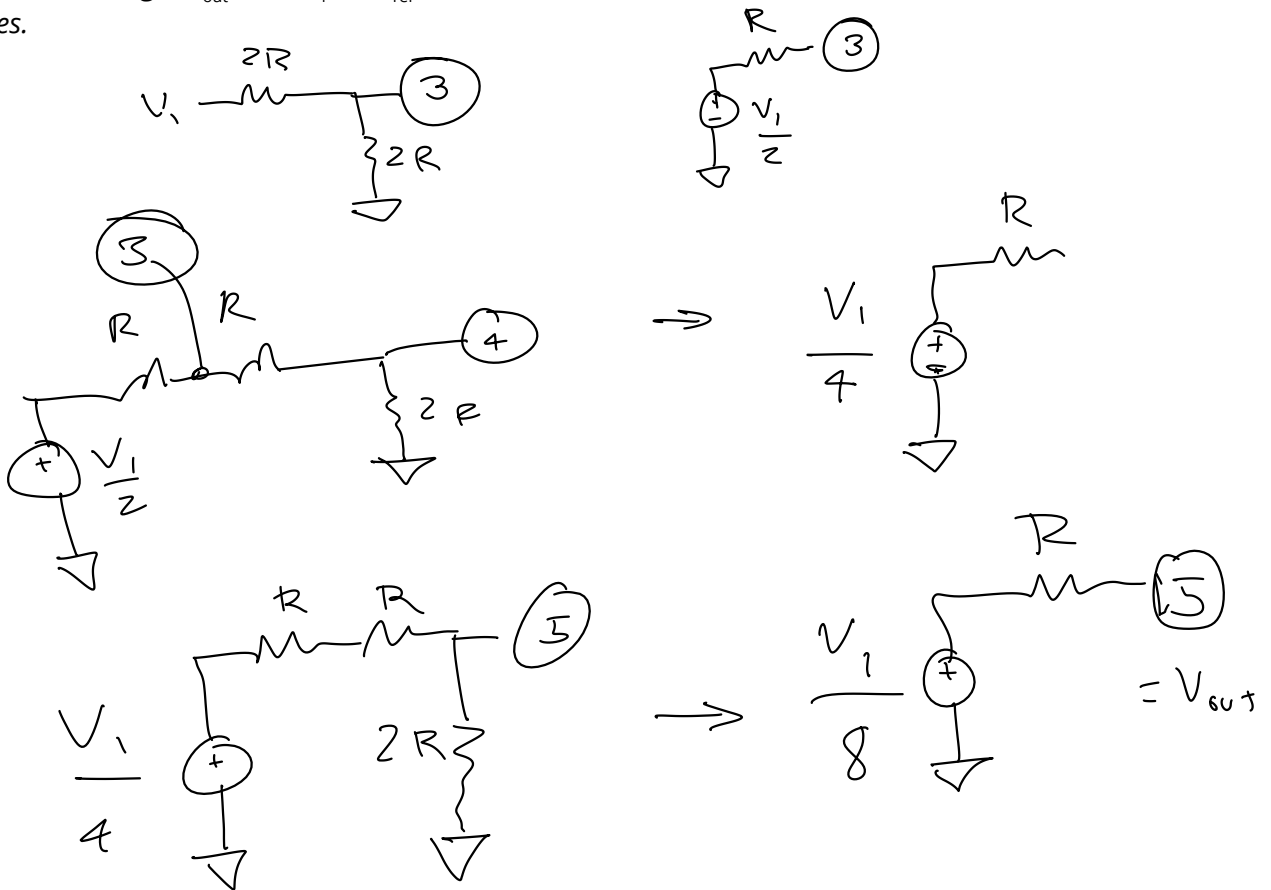
$$\text{ENOB} = n = 3 \text{ bits}$$

$$1.76 + 24.6 = 146 \text{ dB}$$

Exercise 7:

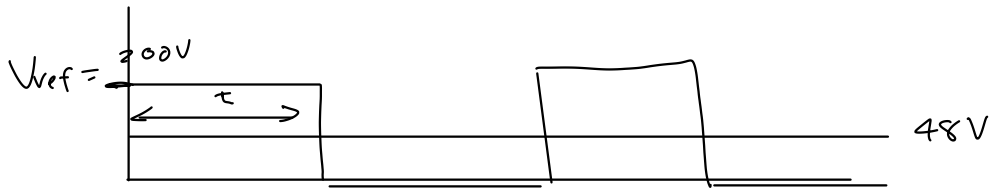


Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenin resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{ref}$). Hint: Do this at the labelled nodes.



Exercise 8: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?

$$V_{out} = V_{ref} \cdot \frac{t}{T}$$

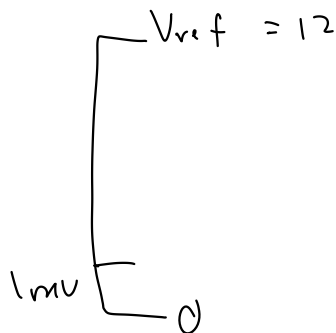


$$T = \frac{1}{25 \text{ kHz}}$$

$$t = \frac{V_{out}}{V_{ref}} \cdot T$$

$$= \frac{48}{200} \cdot \frac{1}{25 \times 10^3} = 9.6 \mu\text{s}$$

Exercise 9: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?



$$2^n \geq \frac{12}{0.001}$$

$$n \geq \log_2(12,000)$$

$$\geq 13$$

$$\text{use } n = 14 \text{ bits}$$



$$T = \frac{1}{10 \text{ kHz}}$$

$$2^n$$

$$T = 2^n T_{\text{clock}}$$

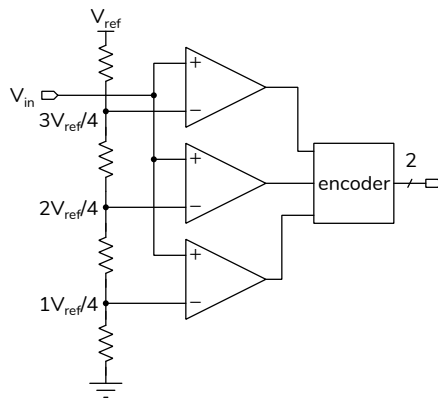
$$T_{\text{clock}} = \frac{T}{2^n} = \frac{100 \mu\text{s}}{2^{14}}$$

$$f_{\text{clock}} = \frac{1}{T_{\text{clock}}} = \frac{2^{14}}{100 \times 10^{-6}} \approx 16.4 \text{ MHz}$$

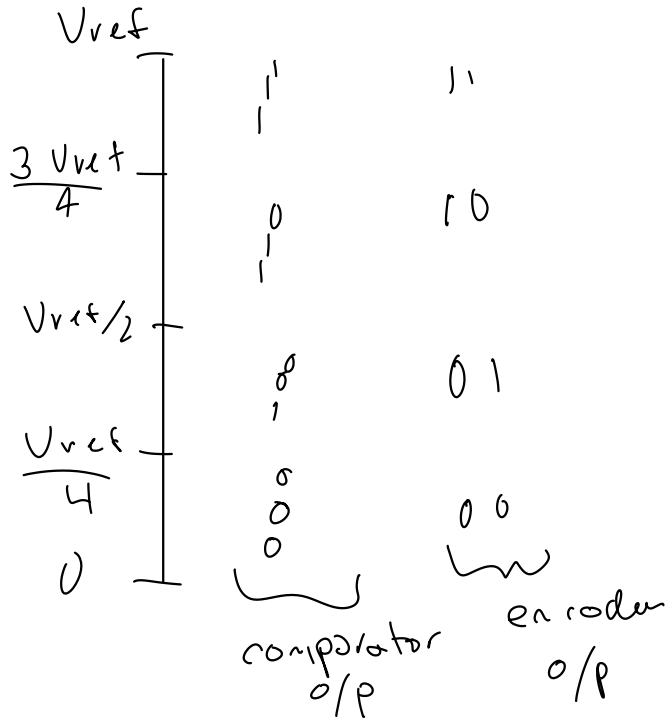
Exercise 10: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

	$\frac{\text{sample rate}}{\text{clock rate}}$	complexity issues
binary weighted	1	resistor matching.
PWM	$\frac{1}{2^n}$	(1 counter) clock rate
$\Sigma-\Delta$	varies	clock rate

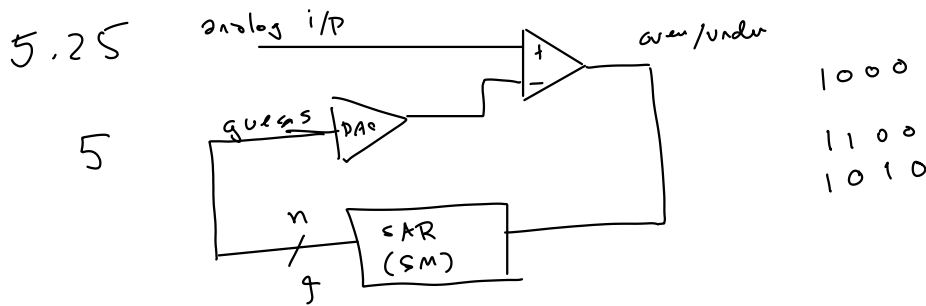
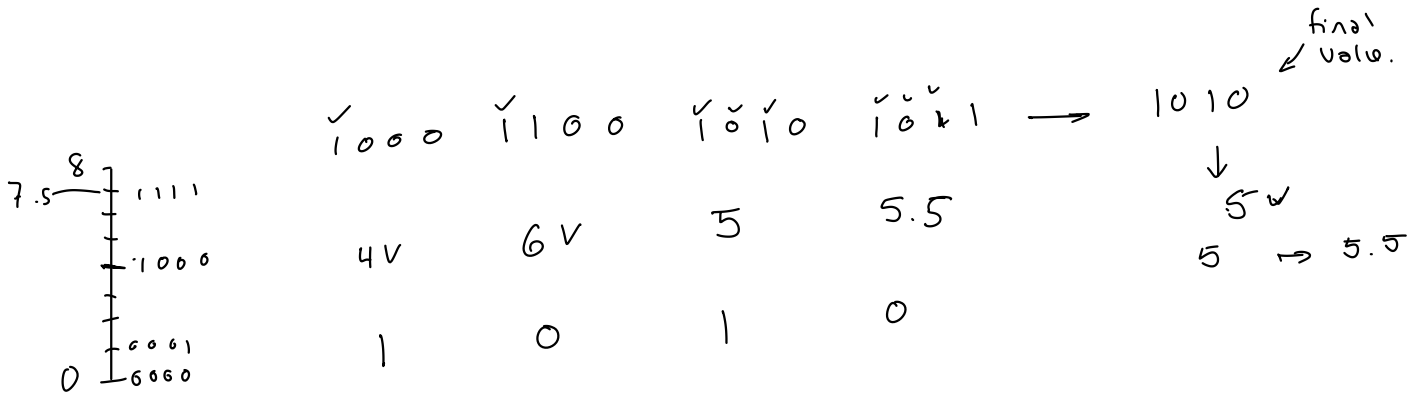
Exercise 11:



Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.



Exercise 12: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output?



Exercise 13: What is the slope of an integrator, in V/s, when charging a 100 nF capacitor with 5 V through a 100 kΩ resistor?

$$C = 100 \times 10^{-9}$$

$$V = 5V$$

$$R = 100 \times 10^3$$

$$Q(t) = CV(t)$$

$$\frac{dQ}{dt} = i = C \frac{dV}{dt}$$

$$\frac{dV}{dt} = \frac{i}{C} = \frac{50 \times 10^{-6}}{100 \times 10^{-9}} = 500 \text{ V/s}$$

