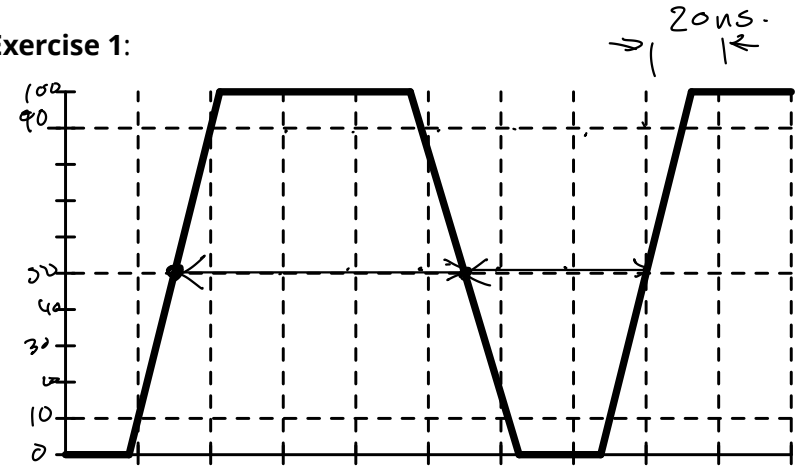
Timing Analysis

Exercise 1:



The diagram above shows an oscilloscope screen capture that includes one period of an *active-low* digital waveform. The scale on the horizontal axis is 20 ns per division. What are: the rise time, period, positive pulse width and duty cycle?

rise time = 20ns.

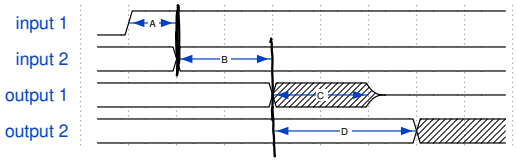
period = 6.5 div · 20 ns/div

= 130 ns.

positive pulse width = 4 · 20 = 80 ns.

$$\text{duty cycle} = \frac{7.5 \cdot 20}{130} = \frac{50}{130} = 38\%$$

Exercise 2:



Label the specifications A through D as requirements or guaranteed responses. Which specifications are measured to a signal being in a high-impedance state? Which are measured from a rising edge only? From either?

A: measured ending on i/p 2 ⇒ req'mnt.

B: " " " o/p 1 ⇒ [guaranteed] response

C: " " " o/p 1 ⇒ response

D: ⇒ response

C is measured to hi-Z (tri-state)

A " " from rising edge only

B, C, D " " " either edge

Exercise 3: Is t_{PD} a requirement or a guaranteed response?

measured to o/p → guaranteed response

Exercise 4: Is t_{SU} a requirement or a guaranteed response? How about t_H?

both are measured to inputs → requirements.

Exercise 5:

$$t_{SU}\text{ (avail)} = T_{clock} - t_{CO}\text{ (max)} - t_{PD}\text{ (max)}$$

Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

t_{co} & t_{PD} decrease t_{su} (avail) as they increase.

T_{clock} increases t_{su} (avail) as it increases.

Exercise 6: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

$f_{clock} = 50\ MHz \rightarrow T_{clock}$ 20ns.

$t_{co} = 2$ ns (max)

$t_{PD} = 15$ ns (max).

t_{su} (req'd) = 5 ns.

t_{su} (avail) → slack.

$$t_{su}(avail) = T_{clock} - t_{co}(max) - t_{PD}(max).$$

$$= 20 - 2 - 15 = 3\ ns.$$

t_{su} (req'd) = 5 ns.

slack = $3 - 5 = -2$ ns.

negative slack ⇒ will not operate reliably

maximum clock frequency is when slack = 0

$\therefore t_{su}(avail) = t_{su}(req'd) = T_{clock} - t_{co} - t_{PD}$

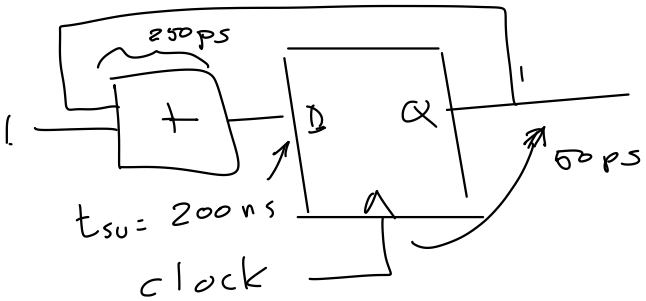
$T_{clock}(min) = t_{su}(req'd.) + t_{co} + t_{PD}$

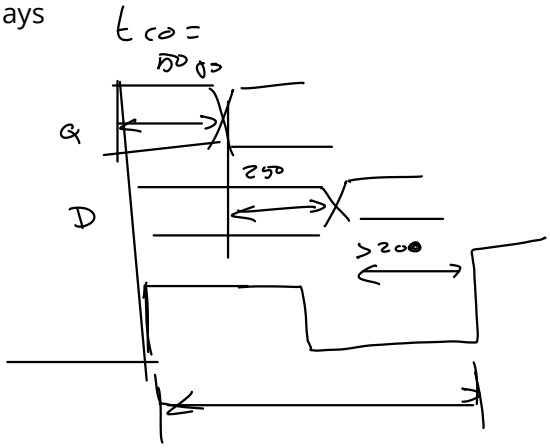
$= 5 + 2 + 15$ ns

$= 22$ ns

$f_{clock}(max) = \frac{1}{22\ ns} = 45\ MHz$

Exercise 7: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps clock-to-output delays and adder logic that has a 250 ps propagation delay?





$T_{clock\,(min)} = 50 + 250 + 200$ ps

$= 500$ ps $=$ 0.5 ns.