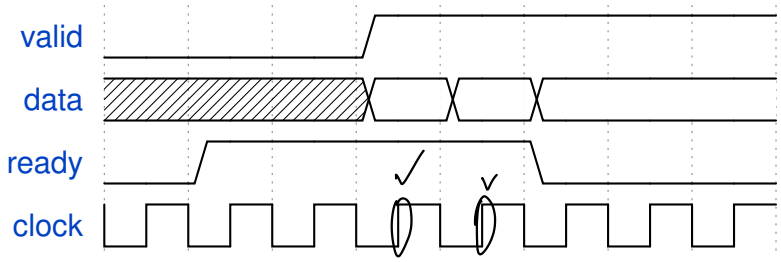
Interfaces

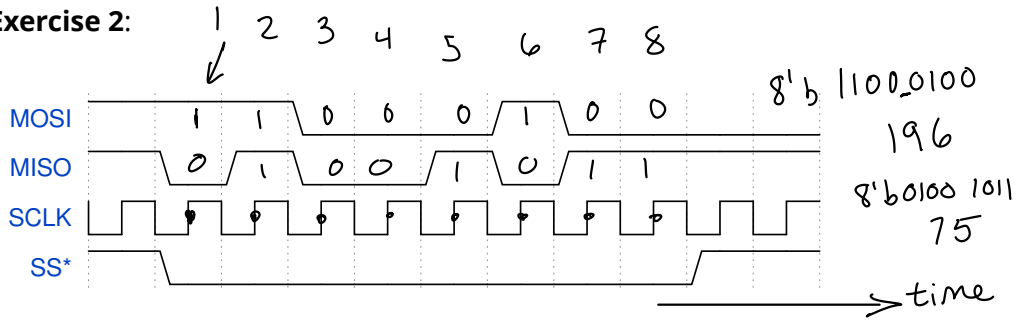
Exercise 1:



Mark the clock edges where data is transferred.

– only when both valid & ready are asserted.

Exercise 2:



The diagram above shows a transfer over an SPI bus. How many bits of data are transferred? What is the value, in decimal, of the data transferred from the master to the slave? From the slave to the master?

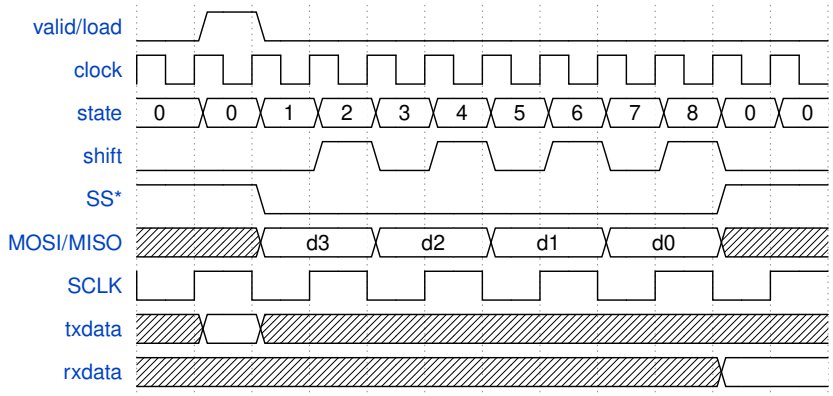
– 8 bits transferred:

$\overline{SS}$ is valid for 8 SCLK rising edges

– master to slave: MOSI = 196

– slave to master: MISO = 75

Exercise 3:



Based on the diagram above, write a state transition table for an SPI interface controller that transfers four bits at a time. Include an idle state. In which states are **SCLK** and $\overline{\text{SS}}$ asserted?

State	valid	next state
0	1	1
8	0	0
8	1	1
n	X	n+1

0 = idle

SCLK asserted in even states (2, 4, 6, 8)

$\overline{\text{SS}}$ asserted in non-zero states (1 to 8).