State Machines

Exercise 1: For the state machine described above, if the current state is 01, what will be the next state? When will the state change? What is the output in state 00? In state 01? In state 10?

Exercise 2: What will be the next state if the state is 00 and the `reset` input is 1? If the state is 00 and the `reset` input is 0? When will the state change? When will the value of `reset` be checked?

Exercise 3: Write the above state transition table using state names A, B, C, and D.

Exercise 4: Modify the diagram so the state machine counts to 11 and stops. Add a down input that cause the values to count down.

Exercise 5: Show the state transition diagram and table for a 2-bit counter with **`reset`**, **`enable`**, and **`down`** inputs. **`reset`** should have priority over **`enable`** which should have priority over **`down`**. Write the Verilog.

Exercise 6: What value of N would result in a 20 ms delay if the clock frequency is 50 MHz? How many bits are needed for this timer's register?

Exercise 7: Assume the timer above is reset to $N - 1$ each time it reaches 0. For how long is the register value 0? What are the period and frequency of a signal that is inverted each time the count reaches 0?

Exercise 8: How many bits need to be considered to detect a specific state when a binary encoding is used? How many need to be considered if a one-hot encoding is used?

Exercise 9: If we used 8-bits of state information, how many states could be represented? What if we used 8 bits of state but used a "one-hot" encoding?