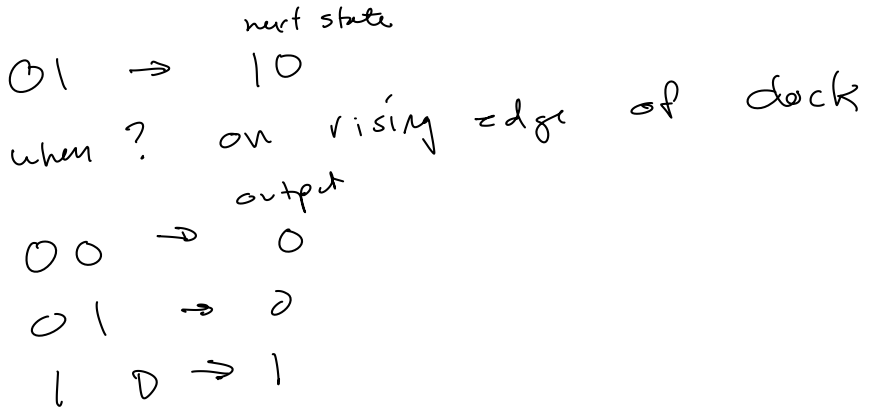
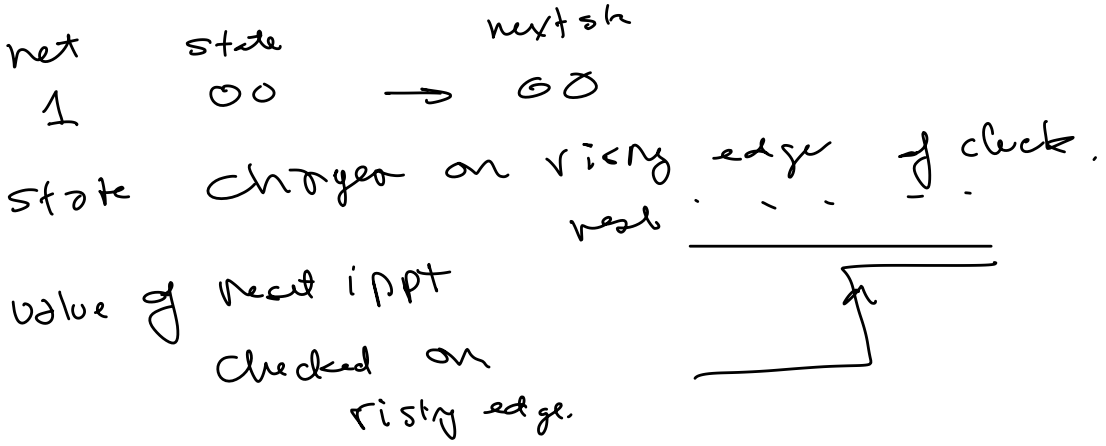
State Machines

Exercise 1: For the state machine described above, if the current state is 01, what will be the next state? When will the state change? What is the output in state 00? In state 01? In state 10?



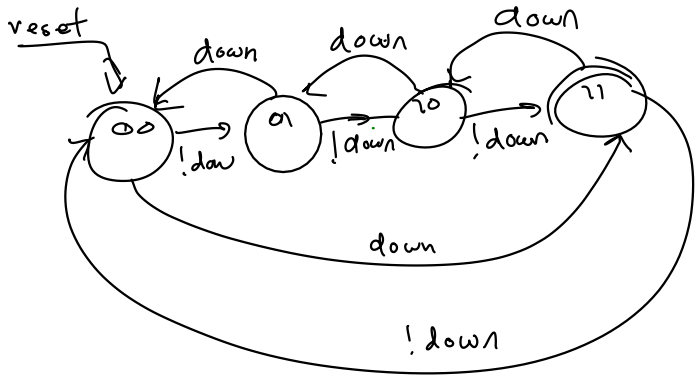
Exercise 2: What will be the next state if the state is 00 and the **`reset`** input is 1? If the state is 00 and the **`reset`** input is 0? When will the state change? When will the value of **`reset`** be checked?



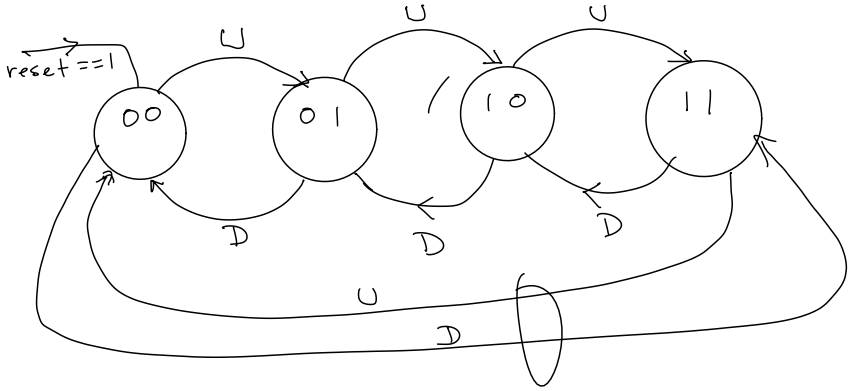
Exercise 3: Write the above state transition table using state names A, B, C, and D.

reset	state	next state
1	xx	A
0	A	B
0	B	C
0	C	D
0	D	A

Exercise 4: Modify the diagram so the state machine counts to 11 and stops. Add a down input that cause the values to count down.



Exercise 5: Show the state transition diagram and table for a 2-bit counter with **`reset`**, **`enable`**, and **`down`** inputs. **`reset`** should have priority over **`enable`** which should have priority over **`down`**. Write the Verilog.



U: enable && !down
D: enable && down

reset	enable	down	count	next count
1	X	X	X X	0 0
0	0	X	n	n
0	1	0	1 1	0 0
0	1	1	0 0	1 1
0	1	0	n	n+1
0	1	1	n	n-1

```
module ex ( input logic clk, reset, enable, down,
            output logic [1:0] count);

always_ff (@ posedge clk) count <=
    reset ? 2'b00 :
    !enable ? count :
    !down && count == 2'b11 ? 2'b00 :
    down && count == 2'b00 ? 2'b11 :
    !down ? count + 1'b1 :
    down ? count - 1'b1 :
    count;
endmodule;
```

Exercise 6: What value of N would result in a 20 ms delay if the clock frequency is 50 MHz? How many bits are needed for this timer's register?

$20\text{ms} = NT \qquad T = \frac{1}{f}$

$= \frac{N}{f}$

$N = f \cdot 20\text{ms} = 50 \times 10^6 \cdot 20 \times 10^{-3} = \underline{1 \times 10^6}$

N-1 ... 0

1 000 000

999 999 ... 0

$2^b - 1 \geq 999\,999$

$2^{10} \approx 1k$

$2^{20} \approx 1M$

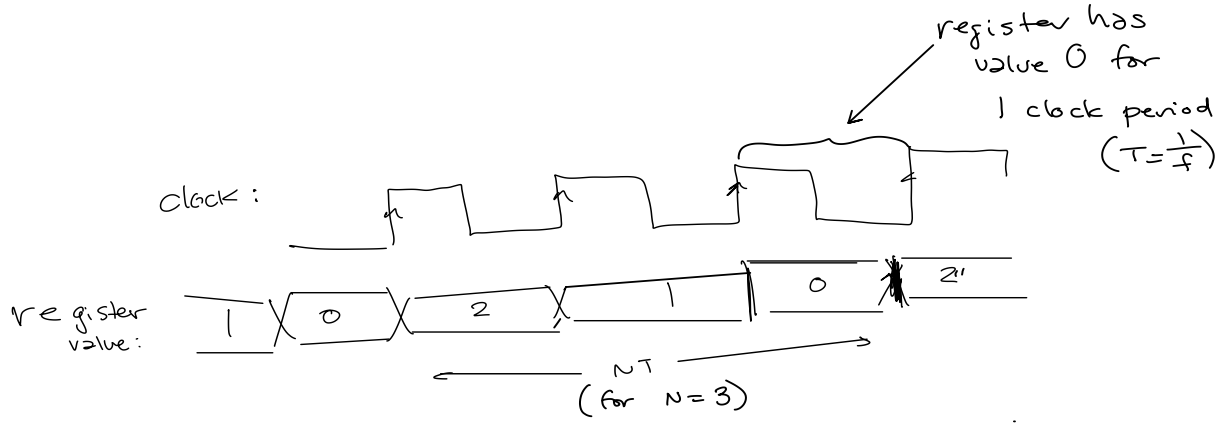
$2^b \geq 10^6$

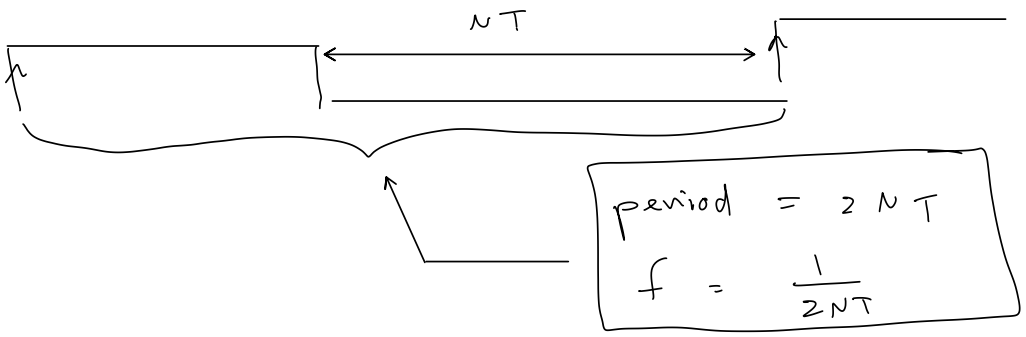
$b \geq \log_2 10^6$

$\geq 19.9\ldots$

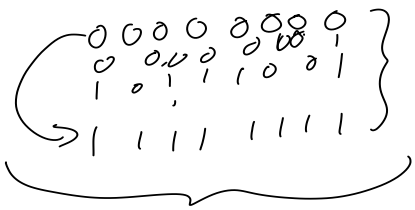
need ceil(19.9) = 20 bits

Exercise 7: Assume the timer above is reset to $N - 1$ each time it reaches 0. For how long is the register value 0? What are the period and frequency of a signal that is inverted each time the count reaches 0?





Exercise 8: How many bits need to be considered to detect a specific state when a binary encoding is used? How many need to be considered if a one-hot encoding is used?



need to check all 8 bits

only need to test one bit

Exercise 9: If we used 8-bits of state information, how many states could be represented? What if we used 8 bits of state but used a "one-hot" encoding?

with 8-bit binary encoding: $2^8 = 256$ states

with one-hot encoding: 8 states