Implementation Technologies

Exercise 1: Would you use hardware or software to implement: A one-off digital clock? A watch whose battery must last for years? A controller for a kitchen appliance? A calculator? An Ethernet interface? For Cryptocurrency "mining"? For an aircraft's automated landing system?

"one-off" — software — for low development cost

battery-powered — hardware for low energy consumption

appliance controller — software — lower overall cost

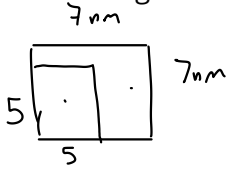
calculator — software — lower development cost

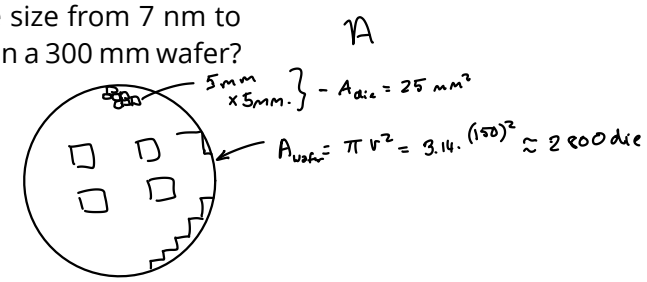
ethernet — hardware — requires many operations per clock

"mining" — hardware — speed & power

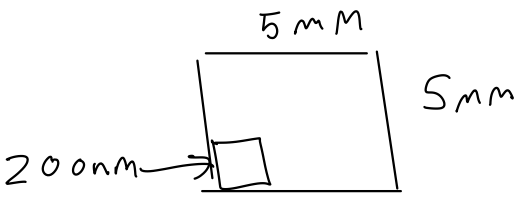
landing system — software? — high reliability required

Exercise 2: What improvement in number of transistors per unit area would be achieved by reducing the feature size from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?





ratio of # xstrs $= \frac{A}{7^2} \div \frac{A}{5^2} = \frac{7^2}{5^2} \approx 2$



$\frac{(5 \times 10^{-3})^2}{(200 \times 10^{-9})^2} \approx 625 \times 10^6$

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

1 month TTM — PLD

100 million units — ASIC

unclear requirements — PLD

CPU — ASIC