Sigma-Delta ADC

Introduction

In this lab you will build a digital voltmeter using a sigma-delta (ΣΔ) ADC. The digital value corresponding to the voltage will be shown on an LED display. You will test your design by comparing the results shown on the LED display to DMM measurements of the same voltage.

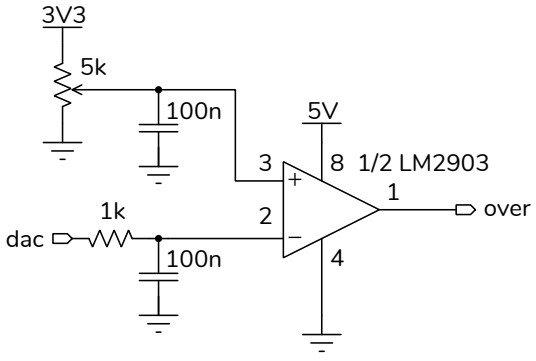
Your design will contain the following modules:

- a top-level module to implement the sigma-delta ADC and instantiate the remaining modules,
- a BCD (binary coded decimal) counter module (provided),
- a clock divider module (provided), and
- a multiplexed LED display module (provided).

You must design the logic for the ADC, integrate it with the supplied code, and demonstrate your design. Block diagrams and descriptions of the ADC are given below.

Circuit

The circuit consists of two counters, a single-bit DAC, an RC low-pass filter ($R = 1\,\text{k}\Omega$, $C = 100\,\text{nF}$, $RC = 100\,\mu\text{s}$), an LM2903 dual analog comparator, and a $5\,\text{k}\Omega$ variable resistor that you can adjust to set the analog input voltage to the ADC:



The LM2903 comparator output is open-collector so a pull-up resistor must be configured on the corresponding CPLD input (named **over**).

Circuit Description

When the voltage on comparator pin 3 is higher than the voltage on pin 2, **over** becomes high. This causes the CPLD to set its **dac** output high. This charges the capacitor on pin 2 and causes this voltage to increase. When this voltage reaches the voltage on pin 3, **over** goes low and the CPLD sets **dac** low as well. This causes the capacitor to discharge until the voltage on pin 2 drops below the voltage on pin 3.

This feedback cycle runs continuously so that the filtered **dac** voltage on pin 2 continuously tracks the analog input voltage on pin 3.

The CPLD measures the average duty cycle of the **dac** output. The voltage on pin 2, and thus on pin 3, is the high-level logic voltage multiplied by the average **dac** waveform duty cycle.

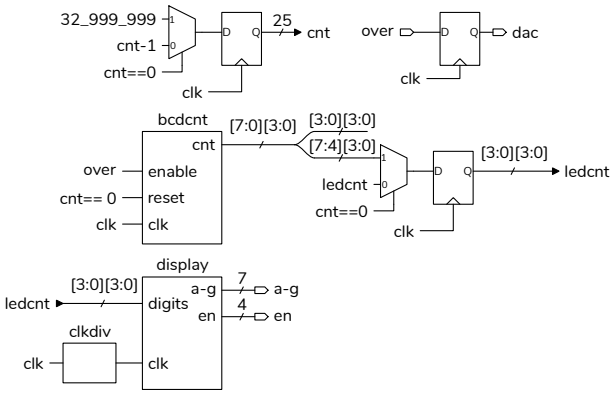
Two counters are used. One counts down from the period (32,999,999 clock cycles) to zero. The other counts the number of clock cycles during this time for which the 1-bit DAC output was high. The average DAC output voltage, and thus the analog input voltage, is equal to the ratio of the two counts times the high-level DAC output.

To allow the voltage to be displayed in millivolts, the number of clock cycles in the measurement interval can be set to be 1000 times the high-level logic voltage. This means the count of **dac** pulses in each measurement interval is equal to the input voltage in millivolts. For example, if the **dac** output was high for 1000 of 3300 clock cycles and the high-level logic level was 3.3 V then the voltage would be $^{1000}/_{3300} \times 3.3 = 1\,\text{V}$.

A BCD counter is used to count **dac** pulses instead of a binary counter. This allows each digit of the count value to be displayed on the LED display without having to convert from binary to decimal.

To reduce the effect of noise, the measurement interval for this lab should be set to 33 million clock cycles. With a 50 MHz clock this results in one measurement every 660 ms. An 8-digit BCD counter is then necessary. Only the most-significant four digits (**[7:4]**) are displayed.

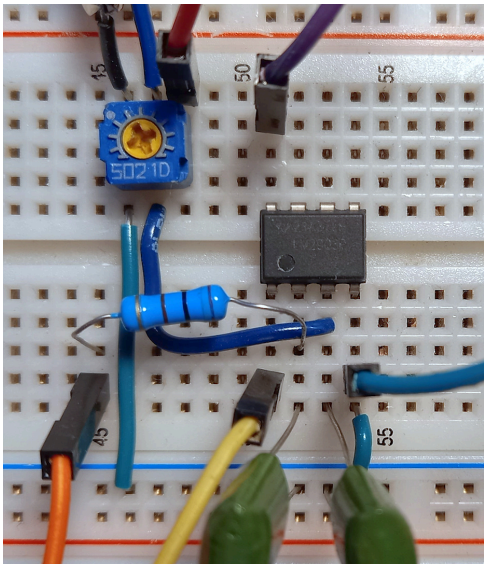
The block diagram below shows the various components:



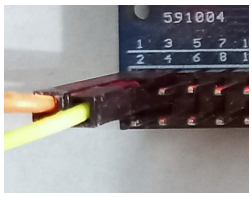
The **bcdcnt**, **display** and **clkdiv** modules are supplied in the **lab8modules.sv** file on the course website. You will need to implement the **cnt** binary counter, the **dac** output flip-flop, and the **ledcnt** register.

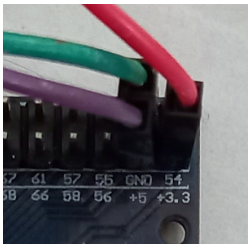
Procedure

Build the circuit shown in the schematic above. For example:



In the sample **.qsf** file **dac** is on pin 1 and **over** is on pin 3, both on connector P1. Connections to +5 V, +3.3 V, and ground are available on the connector P3 on the top right of the board:





Add the code required to implement the ADC described above to the **lab8.sv** file, compile your design, and program the CPLD.

Connect a 4-digit, 7-segment LED display to the **a-g** and **en** outputs as in previous labs.

Connect the CPLD and power it on. Adjust the variable resistor as you measure the DC voltage with a DMM at pin 3 of the comparator. You should be able to adjust the voltage from 0 to 3.3 V.

The LED display should show the measured voltage in millivolts.

Report

Submit a report to the appropriate assignment folder, in PDF format, that includes the following:

- A listing of your Verilog code. Follow the course coding guidelines.
- A compilation report similar to:

Flow Status	Successful - Sat Apr 1 14:09:43 2023
Quartus Prime Version	22.1std.0 Build 915 10/25/2022 SC Lite Edition
Revision Name	lab10
Top-level Entity Name	lab10
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	187 / 240 (78 %)
Total pins	14 / 80 (18 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

- The schematic generated from Tools > RTL Netlist such as that in Figure 1.

If you do not demo your circuit in the lab, submit a video to the appropriate assignment folder showing both the LED and DMM results simultaneously as you adjust the input voltage from 0 to 3.3 V. An example video is available on the course website. Ensure both displays are oriented right-side-up.

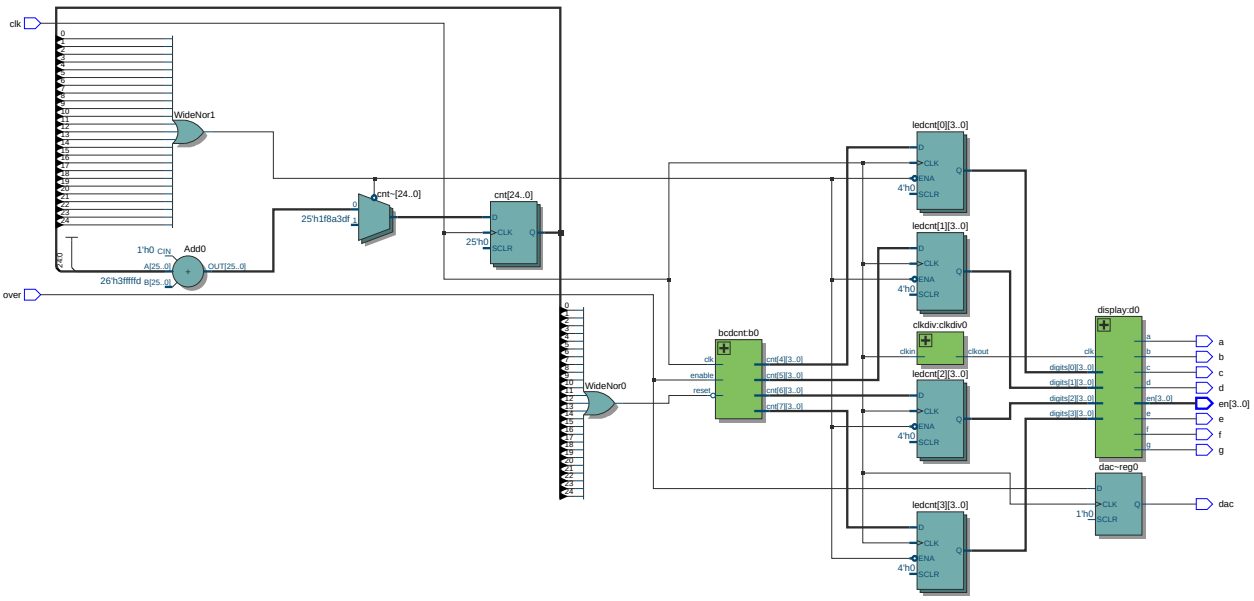


Figure 1: Synthesis results generated by Quartus.

Hints

Measuring the comparator inputs and outputs with a 'scope or DMM may help you narrow down any problems.