Timers and Clock Dividers

Introduction

Counters can be used to create delays and periodic signals (clock dividers).

In this lab you will design a circuit that uses counters to generate an audible tone burst by switching the voltage applied to a speaker on and off for a specific duration.

Your counters will use the 50 MHz clock on the CPLD board. The period of this clock is $1/50\times10^6 = 20$ ns.

Components

You will need:

- your CPLD board, Byte Blaster JTAG interface and mini-USB power connector,
- the matrix keypad
- the speaker from your ELEX 2117 parts kit
- jumpers (or cables with alligator clips on both ends from your ELEX 1117 parts kit[1])

Requirements

You must customize your design using the last three digits of your BCIT ID: n_1, n_2, and n_3. For example, if your BCIT ID is A00123$\boxed{4}\boxed{5}\boxed{6}$ then $n_1 = \boxed{4}$, $n_2 = \boxed{5}$ and $n_3 = \boxed{6}$. Design your circuit so that:

1. keypad key $\boxed{n_1}$ starts the tone,
2. the frequency of the tone is $f = 500 + n_2 \times 100$ Hz,
3. the tone lasts for $1 + n_3/3$ seconds.

For example, for an ID ending in 456, pressing keypad $\boxed{4}$ should generate a $500 + \boxed{5} \times 100 = 1000$ Hz tone for $1 + \boxed{6}/3 = 3$ seconds.

The tone should last for the required duration even if the key is released before the end of the tone duration.

[1] You can put alligator clips over the banana plugs.

Hints

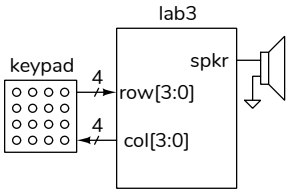
You can design this circuit using a timer and a clock divider:

- The timer is a counter that counts from $M-1$ down to zero each time the appropriate key is pressed. The counter is set to $M-1$ when the appropriate key is pressed AND the count value is zero. Otherwise, if the counter is not zero, it is decremented by 1. Otherwise the count is unchanged (left at 0). The duration of the timer is MT where T is the clock period.
- The clock divider is a counter that continuously counts from $N-1$ down to 0. The clock divider's counter is set to $N-1$ when this counter reaches zero, otherwise it is decremented by 1. The period of this counter will thus be NT where T is the clock period.

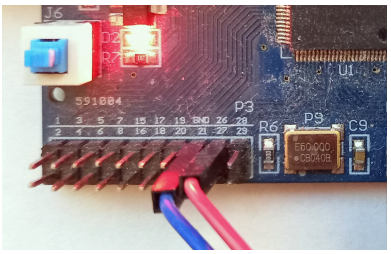
If you set the speaker output high when the timer's counter value is non-zero and the clock divider's counter value is greater than $N/2$ then the speaker output value will be a square wave of the appropriate period and duration.

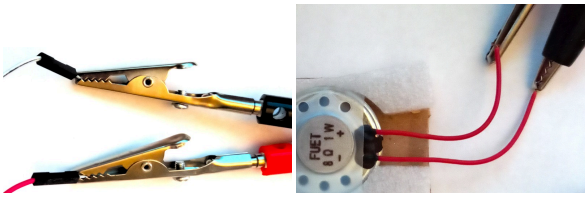
CPLD I/O

The following diagram shows the connections to the CPLD:



Connect the matrix keypad to the CPLD as in previous labs. Connect a CPLD I/O pin to the speaker pin and a ground pin with alligator clip cables (pin 26 was used as the **spkr** pin here, a ground pin is next to it):





Procedure

Create a project, compile it, and configure the CPLD.

If you use the same keypad pins as in the previous lab and Pin 26 for the speaker output, you should end up with the following pin assignments:

tatu	From	To	Assignment Name	Value	Enabled	
✔		row[3]	Location	PIN_99	Yes	
✔		row[2]	Location	PIN_97	Yes	
✔		row[1]	Location	PIN_95	Yes	
✔		row[0]	Location	PIN_91	Yes	
✔		col[3]	Location	PIN_89	Yes	
✔		col[2]	Location	PIN_87	Yes	
✔		col[1]	Location	PIN_85	Yes	
✔		col[0]	Location	PIN_83	Yes	
✔		clk50	Location	PIN_12	Yes	
✔		spkr	Location	PIN_26	Yes	
✔		led	Location	PIN_77	Yes	
✔		row	Weak Pull-Up Resistor	On	Yes	lab3
	<<new>>	<<new>>	<<new>>			

You can import these pin assignments above from the **`lab3.qsf`** file on the course website.

For troubleshooting you can assign internal signals to the **`led`** output on pin 77 . A high level turns on this on-board LED. You can also view this signal with an oscilloscope.

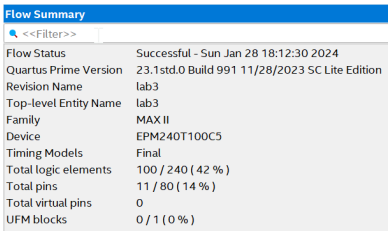
Test your design.

Submission

To get credit for completing this lab, submit the following to the appropriate Assignment folder on the course website:

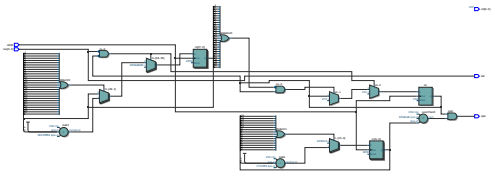
- A PDF document containing:

  1. (a) The values of n_1, n_2, and n_3 corresponding to your BCIT ID.
     (b) The corresponding button to be pushed, tone frequency and duration.
     (c) The value of **`row`** for your value of n_1.
     (d) The values of N and M for your values of n_2, and n_3.
     (e) A block diagram of your solution. Follow the instructions in the report and video guidelines document.
  2. A listing of your Verilog code.
  3. A screen capture of your compilation report (**Window > Compilation Report**) similar to:



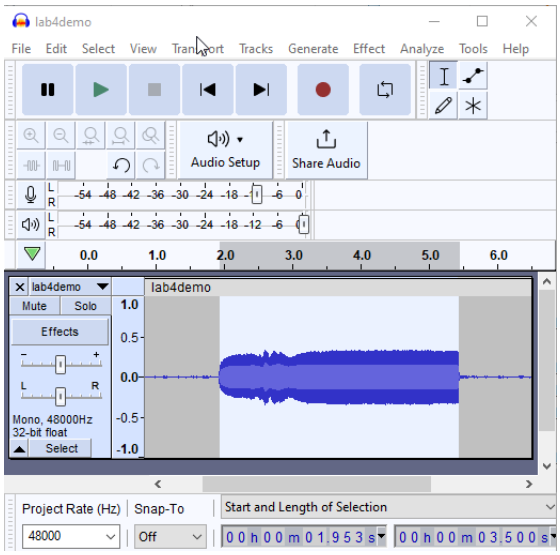
Flow Summary	
<<Filter>>	
Flow Status	Successful - Sun Jan 28 18:12:30 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	MAX II
Device	EPM240T100C5
Timing Models	Final
Total logic elements	100 / 240 (42 %)
Total pins	11 / 80 (14 %)
Total virtual pins	0
UFM blocks	0 / 1 (0 %)

  4. The schematic created by **Tools > Netlist Viewers > RTL Viewer** and then **File > Export...**. For example:



- If you did not demonstrate your completed lab in person, submit a short video, including audio, showing: (1) the tone generated by a button press *shorter* than the tone duration, and (2) that no tone is generated when pressing a button on a different row and a different column. The audio should be clearly audible so that the instructor can check the duration and frequency of your tone. A sample video is available on the course website.

  Optionally, you can check the tone duration and frequency using an audio editor such as Audacity. For example, here is a display of a recorded audio waveform showing that the selected portion has a duration of 3.5 seconds:



and a plot of the spectrum (Analyze/Plot Spectrum...) showing the fundamental frequency at 1000 Hz and the odd harmonics (at 3, 5, ... kHz):