Combinational Logic Design with Verilog

Introduction

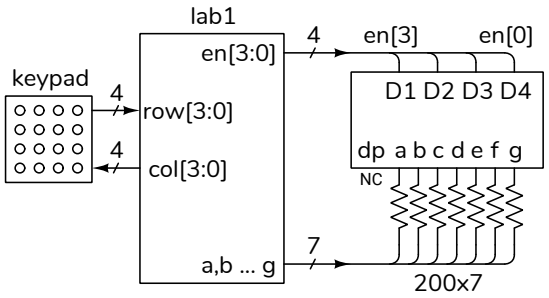
In this lab you will connect a 4x4 matrix keypad and a 4-digit, 7-segment LED display to the CPLD board. You will write a Verilog module to display one of the last three digits of your student number on the rightmost LED digit depending on which keypad button is pressed.

You will need the components used in the previous lab (CPLD board and USB-Blaster) plus the following:

- solderless breadboard (from previous course)
- 11 M-F ("Dupont" or "Berg") pin-header jumpers (from previous course)
- 4×4 matrix keypad
- seven (7) 200 Ω resistors
- an FJ5463AH 4-digit, 7-segment common-cathode LED display

Circuit Description

The following diagram shows how the keypad and LED are connected to the CPLD and the recommended signal names:



Your circuit should display one of the last three digits of *your* BCIT ID in the rightmost digit position when the keypad buttons 1, 4, and 7 are pressed. For example, if your BCIT ID is A00123456 then when button 1 is pressed the rightmost LED should display 4, when button 4 is pressed the rightmost LED should display 5, and when button 7 is pressed the rightmost LED should display 6. All other conditions should result in a blank display.

Component Connections

CPLD Board

The CPLD has 100 pins. Seventy-six (76) of these are available on four 20-pin headers and will be used to connect components such as the LED display and keypad. The CPLD pin numbers are marked on the PCB. The remaining four header pins provide two grounds, a 3.3 V, and a 5 V supply.

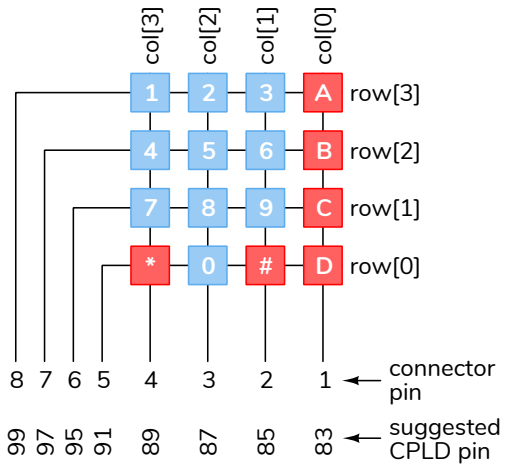
The CPLD's I/O pins use 3.3V logic levels. To avoid damaging the board:

> **Never connect your circuits to an external power supply or use the on-board 5V supply.**

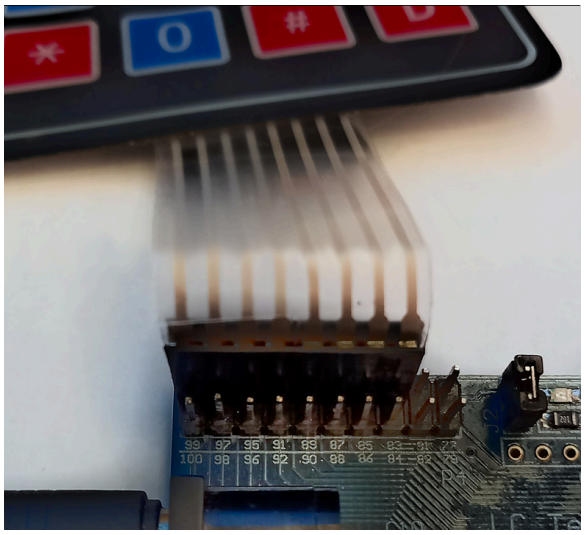
4x4 Matrix Membrane Keypad

The keypad consists of two plastic sheets with conductive traces. One has horizontal traces and the other has vertical traces. The sheets face each other and are separated by spacers. Pressing the keypad in a digit locations connects the corresponding row and column traces.

The diagram below shows the suggested HDL signal names and the suggested CPLD pin numbers used to connect the keypad. You may use different pins; for example, if some of your IO pins are damaged.



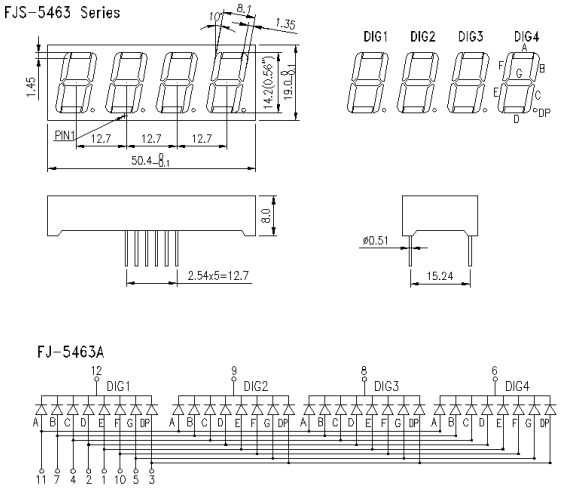
The photo below shows how the keypad is connected:



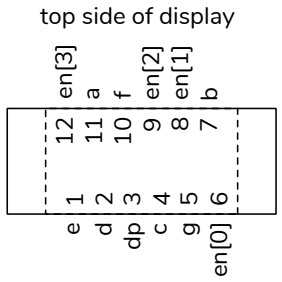
To detect button presses on matrix keypads the columns are connected to outputs and the rows to inputs. In this lab the left column will be set low and the others columns will be set high. The row inputs will be pulled high by an internal (to the CPLD) pull-up resistor. Pressing a button along the left column will connect the low logic output on the left column to one of the row inputs which will drive it low. For example, `row` will be `4'b1111` when no button is pushed and will be `4'b1110` when button `*` is pressed.

4-digit, 7-segment Multiplexed LED Display

The datasheet for the multiplexed, 4-digit, 7-segment LED display included in your parts kit is shown below:



The display pinout is:

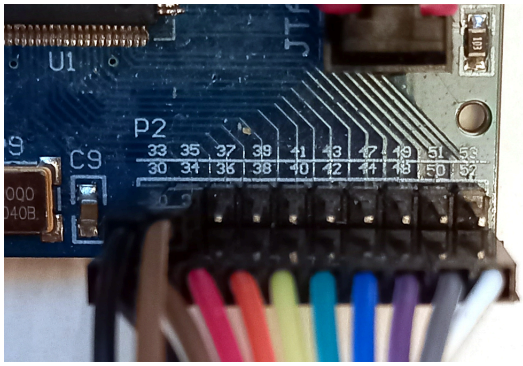


Review the schematic above and notice how the LEDs are connected. This is a common-cathode display so you must set the pin for a segment (A-G) high and the desired digit enable (DIG1 through DIG4) low to turn on that LED segment. Note that only one digit can be displayed at a time.

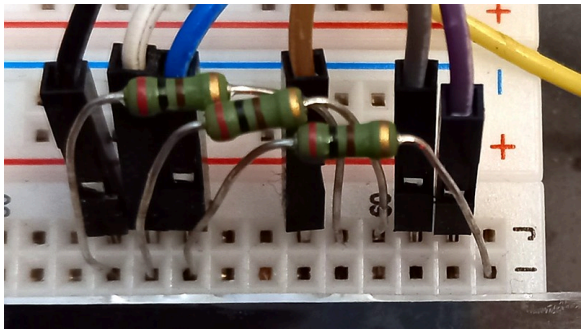
The table below shows one way to connect the CPLD to the display. Note the use of colour coding.

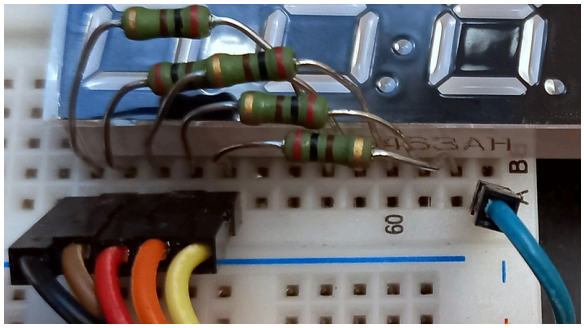
LED Pin	wire colour	segment	CPLD pin
1	black	e	30
2	brown	d	34
3	red	dp	36
4	orange	c	38
5	yellow	g	40
6	green	en[0]	42
7	blue	b	44
8	violet	en[1]	48
9	gray	en[2]	50
10	white	f	52
11	black	a	33
12	brown	en[3]	35

The photo below shows the connections to the CPLD pins:



and the photos below shows the connections to the LED on the breadboard.





The active-low[1] digit-enable outputs are named **en[3]** through **en[0]** in order from left to right and the active-high segment-enable outputs are **a** through **g** (see the diagram above). For this lab only the rightmost digit is used so (**en[0]**) needs to be set low and the other digit enables high.

The segments are connected through 200 Ω resistors to avoid exceeding the CPLD's maximum current specification. The four common cathodes are connected directly.

[1] "Active-low" means an input or output is at a low logic level when it's true. A button would be considered "true" when pressed and an LED segment "true" when lit.

Procedure

Follow the general procedure in the Software Installation and Use document on the course website to create a project, compile it and configure the CPLD. Connect the CPLD board to the keypad and LED. Test your design and fix any errors.

As an example, the following truth table shows the values of the **row** input, the displayed LED digit and the values of segments a through g for an ID of A00123456:

button	row	display	a...g
none	4'b1111		7'b000_0000 (7'h00)
1	4'b0111	4	7'b011_0011 (7'h33)
4	4'b1011	5	7'b101_1011 (7'h5b)
7	4'b1101	6	7'b101_1111 (7'h5f)

Internal Pull-Up Resistors

When you assign signals to pins you'll also need to configure internal pull-up resistors on the four **row** input pins. Open the Assignment Editor (**Assignments > Assignment Editor**). Double-click on «new». in the **To** column and enter the (bus) name (**row**). Select **Weak Pull-Up Resistor** from the drop-down menu in the **Assignment Name** column. Select **On** from the drop-down menu in the **Value** column.

If you used the pin assignments above you should end up with the following:

To	Assignment Name	Value
clk50	Location	PIN_12
row[3]	Location	PIN_99
row[2]	Location	PIN_97
row[1]	Location	PIN_95
row[0]	Location	PIN_91
e	Location	PIN_30
d	Location	PIN_34
dp	Location	PIN_36
c	Location	PIN_38
g	Location	PIN_40
en[0]	Location	PIN_42
b	Location	PIN_44
en[1]	Location	PIN_48
en[2]	Location	PIN_50
f	Location	PIN_52
a	Location	PIN_33
en[3]	Location	PIN_35
col[3]	Location	PIN_89
col[2]	Location	PIN_87
col[1]	Location	PIN_85
col[0]	Location	PIN_83
row	Weak Pull-Up Resistor	On

Hints

1. You can use the Verilog concatenation operator (`{,}`) on the left-hand side of an assignment. For example:

```
...
   assign {a,b,c,d,e,f,g}
     = row == 4'b1011 ? 7'h5b :
...
```

2. To save you time, here are the active-high seven-segment values (`a` to `g`) for digits 0 to 9 in order from most- to least-significant bit[2]:

```
0  7'h7e
1  7'h30
2  7'h6d
3  7'h79
4  7'h33
5  7'h5b
6  7'h5f
7  7'h70
8  7'h7f
9  7'h7b
```

3. We'll be using the same display in later labs. Leave the LED, resistors and wires connected to your CPLD if you can (if necessary, a small extra breadboard might be worthwhile).

4. You may want to use ModelSim to check your code for syntax errors – it compiles much faster.

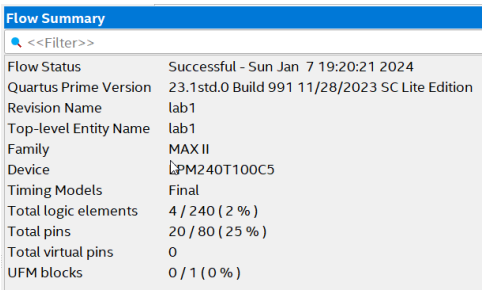
5. Build and test a little bit at a time. For example, you could start by checking that you can detect keypad button presses by using a column input to turn the on-board LED on and off. Then you could check that you can display one digit of your ID.

Lab Report

Submit the following to the appropriate Assignment folder on the course website:

1. A PDF document containing:

   - A block diagram of your design. Label all signals. Use multiplexers for conditional operators and Verilog expressions for other logic. Use Verilog syntax for numeric literals.
   - A listing of your Verilog code.
   - A screen capture of your compilation report, for example:



2. If you were not able to demonstrate your solution to the lab instructor during your lab period, submit a video showing the keypad and the LED display as you push the four keypad buttons on the left column from top to bottom and the buttons `5`, `9` and `D`. The rightmost LED should display the last three digits of *your* BCIT ID.

> Follow the *Report and Video Guidelines* and *Coding Guidelines* documents on the course website.

[2] From Wikipedia.