ELEX 2117 : Digital Techniques 2
2024 Winter Term

Solutions to Final Exam

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

Write a Verilog module named **fastcount** (or **slowcount**) that has three one-bit inputs named **clk**, **reset**, and **fast** (or **slow**), and an 20-bit output named **count**.

count changes only on the rising edge of **clk**. If **reset** is asserted then **count** is set to 0. Otherwise **count** is incremented by 16 (or 1) if **fast** (or **slow**) is asserted, otherwise it is incremented by 1 (or 16) .

Follow the course coding conventions but omit comments.

Answers

Solutions to the two versions of the question, a testbench, and simulation results are shown below and in Figure 1.

```
module fastcount
  ( input logic clk, reset, fast,
    output logic [19:0] count) ;

   always_ff @(posedge clk) count
     <= reset ? '0 :
        fast ? count + 20'd16 : count + 20'd1 ;

endmodule

module slowcount
  ( input logic clk, reset, slow,
    output logic [19:0] count) ;

   always_ff @(posedge clk) count
     <= reset ? '0 :
        slow ? count + 20'd1 : count + 20'd16 ;

endmodule

module tb ;
   logic clk, reset, slow, fast ;
   logic [19:0] count1, count2 ;

   slowcount s0 (.count(count1),.*) ;
   fastcount f0 (.count(count2),.*) ;

   initial begin
      $dumpfile("exam1.vcd") ; $dumpvars()  ;
      {clk,reset,slow,fast} = {4'b0100} ;
      #2 reset = '0 ;
      #4 {slow,fast} = '1 ;
      #6 $finish ;
   end

   always #1 clk = !clk ;

endmodule
```

Question 2

Fill in the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that **x** has the value **8'hd6** (or **8'h49**) and that **y** has the value **4'ha** (or **4'h5**). The first row has been filled in as an example.

expression	value
x[3:0]	4'h6 (or 4'h9)
x[3:0] | y	
{ x[7:1], y>7 }	
x << y - 1	
{ ~y, 4'b1 }	
y >= 7 ? ! y : y + 1'b1	

Answers

expression	value
x[3:0]	4'h6
x[3:0] | y	4'he
{ x[7:1], y>7 }	8'hd7
x << y - 1	8'h0
{ ~y, 4'b1 }	8'h51
y >= 7 ? ! y : y + 1'b1	4'h0

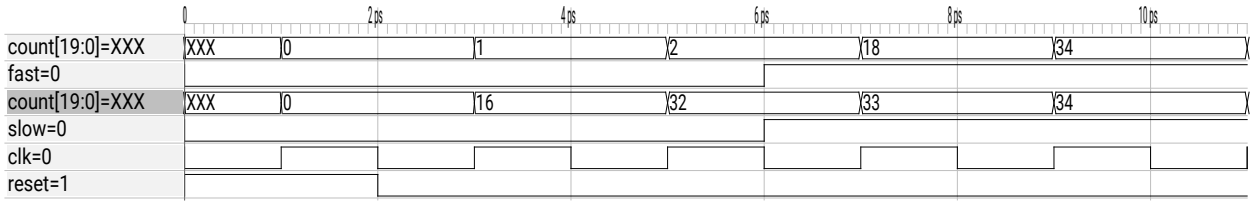
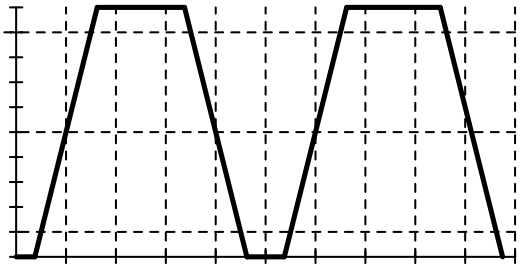


Figure 1: Simulation waveforms for Question 1.

or:

expression	value
`x[3:0]`	`4'h9`
`x[3:0] | y`	`4'hd`
`{ x[7:1], y>7 }`	`8'h48`
`x << y - 1`	`8'h90`
`{ ~y, 4'b1 }`	`8'ha1`
`y >= 7 ? ! y : y + 1'b1`	`4'h6`

Question 3



The diagram above shows an oscilloscope screen capture that includes one period of an *active-high* digital waveform. The scale on the horizontal axis is 25 (or 5) ns per division. What are the values of the following? Include units and give your answers in nanoseconds or percent, as appropriate.

(a) rise time:

(b) period:

(c) positive pulse width:

(d) duty cycle:

Answers

The number of divisions and the values for the two timescales are given below.

(a) rise time: 1 division $\times$ 25 = $\boxed{25\text{ ns}}$ (or $\boxed{5\text{ ns}}$)

(b) period: 5 divisions $\times$ 25 = $\boxed{125\text{ ns}}$ (or $\boxed{25\text{ ns}}$)

(c) positive pulse width: 3 divisions $\times$ 25 = $\boxed{75\text{ ns}}$ (or $\boxed{15\text{ ns}}$)

(d) duty cycle: 3/5 divisions = $\boxed{60\%}$

Question 4

A synchronous digital logic circuit has a maximum propagation delay through any combinational logic path of 10 (or 4) ns. The registers in this circuit have a clock-to-output delay of 5 ns (or 0.5 ns) and a minimum required setup time of 5 ns (or 0.5 ns). What is the maximum clock rate at which this circuit will operate reliably?

Answers

In the equation for the available setup time:

$$t_{SU}(\text{avail}) = T_{clock} - t_{CO}(\text{max}) - t_{PD}(\text{max})$$

The slack is zero at the maximum clock rate and we can substitute:

$$t_{SU}(\text{avail}) = t_{SU}(\text{required})$$

and solve for T_{clock}:

$$\begin{aligned} T_{clock} &= t_{CO}(\text{max}) + t_{PD}(\text{max}) + t_{SU}(\text{required}) \\ &= 5 + 10 + 5(\text{or} 4 + 0.5 + 0.5) \\ &= 20\text{ ns or }5\text{ ns} \end{aligned}$$

From which the maximum clock rate is $f = 1/T =$ $\boxed{50\text{ MHz}}$ (or $\boxed{200\text{ MHz}}$).

Question 5

A state machine has two inputs named **a** and **b**. Its state can be represented as a two-bit value. The state transition table for the state machine is shown below and follows the conventions used in the lecture notes.

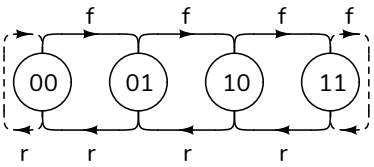
Draw the state transition diagram for this state machine. Follow the conventions shown in the lecture notes for state transition diagrams. *Hint: Label the state transitions unambiguously.*

State	a	b	Next State
00	0	1	01
00	1	0	00
01	0	1	10
01	1	0	00
10	0	1	11
10	1	0	01
11	0	1	11
11	1	0	10

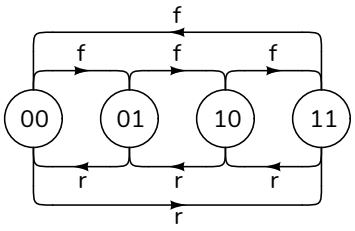
or:

State	a	b	Next State
00	0	1	01
00	1	0	11
01	0	1	10
01	1	0	00
10	0	1	11
10	1	0	01
11	0	1	00
11	1	0	10

Answers



or:



f: !a && b
r: a && !b

---- :optional

Question 6

An IC has the following logic level specifications:

Table 5–5. 3.3-V LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.75	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.75	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(1)*	2.25		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(1)*		0.25	V

or:

Table 5–5. 3.3-V LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.5	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.65	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(1)*	2.6		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(1)*		0.35 V	

(a) What is the noise margin for a high logic level?

(b) What is the noise margin for a low logic level?

Answers

- For the high logic level the noise margin is: $V_{OH(min)} - V_{IH(min)} = 2.25 - 1.75 = \boxed{0.5\,V}$
- For the low logic level the noise margin is: $V_{IL(max)} - V_{OL(max)} = 0.75 - 0.25 = \boxed{0.5\,V}$

or:

- For the high logic level the noise margin is: $V_{OH(min)} - V_{IH(min)} = 2.6 - 1.5 = \boxed{1.1\,V}$
- For the low logic level the noise margin is: $V_{IL(max)} - V_{OL(max)} = 0.65 - 0.35 = \boxed{0.3\,V}$

Question 7

(a) What clock rate would be required to implement an 8 (or 12)-bit SAR ADC operating at a sampling rate of 64 kHz?

(b) The signal to noise ratio at the output of a DAC is 66 (or 72) dB. The noise includes quantization noise and other effects such as distortion. What is the effective number of bits (ENOB)?

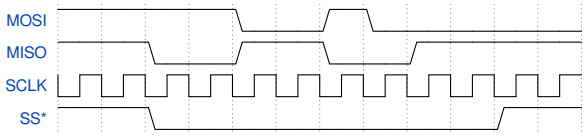
Answers

(a) A SAR ADC requires one clock cycle per bit of resolution. Thus the required clock rate would be 8 (or 12) times the sampling rate of 64 kHz: $\boxed{512\text{ kHz}}$ (or $\boxed{768\text{ kHz}}$).

(b) The ENOB is the number of bits required to produce a quantization SNR equal to the measured SNR. This is $1.76 + 6B$ dB. For an SNR of 66 (or 72) dB, $B = (66 - 1.76)/6 = \boxed{10.7\text{ bits}}$ (or $(72 - 1.76)/6 = \boxed{11.7\text{ bits}}$.

Question 8

The waveforms below show a data transfer over an SPI interface. The interface follows the conventions described in the lecture notes.

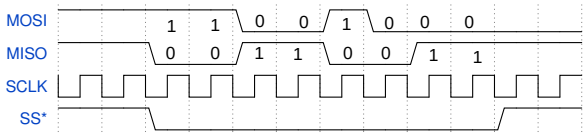


(a) How many bits were transferred?

(b) What numerical value was transferred from the master to the slave (or from the slave to the master) Give your answer as a hexadecimal number.

Answers

Bits are transferred to the slave on MOSI and to the master on MISO on each (rising) clock edge when $\overline{\text{SS}}$ is low. The following figure shows the values of the bits transferred on each clock edge:



(a) Eight $\boxed{8}$ bits were transferred in each direction.

(b) The value was transferred is $\boxed{\text{C8}}$ in hexadecimal (1100 1000 binary) from the master to the slave on MOSI and $\boxed{33}$ (0011 0011 binary) from the slave to the master on MISO.

Question 9

A digital circuit operating at 30 MHz consumes 200 mW (or 100 mW). What clock rate would allow this circuit to operate for one year from a 3000 mW-h (milliwatt-hour) battery? *Hint: A year is approximately 3000 hours.*

Answers

The capacity of a battery, measured in mW-hours, is the product of the power supplied by the battery and the duration over which this power is supplied ($C = P \cdot T$). In this problem $T = 3000$ (although the true value is 365.25 days/year × 24 hours/day = 8766 hours/year) and $C = 3000$ mW-h. Thus the maximum power that could be supplied continuously for one year is $3000/3000 = 1$ mW (the true value is $3000/8766 = 0.342$ mW).

Power consumption for a CMOS circuit, by far the most common technology used today, is approximately proportional to the clock rate:

$$\frac{P_2}{P_1} = \frac{f_2}{f_1}$$

In this case $P_1 = 200$ mW (or 100 mW), $P_2 = 1$ mW, and $f_1 = 30$ MHz. Solving for the required clock rate:

$$\begin{aligned} f_2 &= f_1 \cdot \frac{P_2}{P_1} \\ &= 30\,\text{MHz} \cdot \frac{1\,\text{mW}}{200\,\text{mW (or 100 mW)}} \\ &= \boxed{150\,\text{kHz}}\ (\text{or}\ \boxed{300\,\text{kHz}}) \end{aligned}$$

Using the actual value for the number of hours per year, the two answers would be scaled by 0.342: $\boxed{51.3\,\text{kHz}}$ (or $\boxed{103\,\text{kHz}}$).

Question 10

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

ready/valid	
ASIC	
FPGA	
feature size	
wafer	
NRE	
LE	

(1) used to manufacture die
(2) custom-designed IC
(3) one-time costs
(4) measured in nanometers
(5) building block of a PLD
(6) PLD
(7) interface

or:

(1) interface
(2) used to manufacture die
(3) building block of a PLD
(4) measured in nanometers
(5) PLD
(6) one-time costs
(7) custom-designed IC

Answers

ready/valid	7
ASIC	2
FPGA	6
feature size	4
wafer	1
NRE	3
LE	5

ready/valid	1
ASIC	7
FPGA	5
feature size	4
wafer	2
NRE	6
LE	3