ELEX 2117 : Digital Techniques 2
2024 Winter Term

FINAL EXAM
14:30-17:30
Monday, April 15, 2024
SW05-1840

This exam has ten (10) questions on four (4) pages. The marks for each question are as indicated. There are a total of thirty-seven (37) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

Write a Verilog module named **`slowcount`** that has three one-bit inputs named **`clk`**, **`reset`**, and **`slow`**, and an 20-bit output named **`count`**.

`count` changes only on the rising edge of **`clk`**. If **`reset`** is asserted then **`count`** is set to 0. Otherwise **`count`** is incremented by 1 if **`slow`** is asserted, otherwise it is incremented by 16 .

Follow the course coding conventions but omit comments.

Question 2 — 5 marks

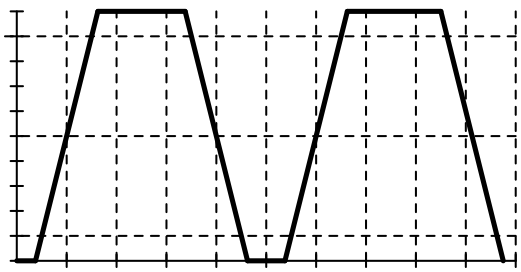
Fill in the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that **`x`** has the value **`8'h49`** and that **`y`** has the value **`4'h5`**. The first row has been filled in as an example.

expression	value
`x[3:0]`	`4'h9`
`x[3:0] | y`	
`{ x[7:1], y>7 }`	
`x << y - 1`	
`{ ~y, 4'b1 }`	
`y >= 7 ? ! y : y + 1'b1`	

Question 3 — 4 marks



The diagram above shows an oscilloscope screen capture that includes one period of an *active-high* digital waveform. The scale on the horizontal axis is 5 ns per division. What are the values of the following? Include units and give your answers in nanoseconds or percent, as appropriate.

(a) rise time:

(b) period:

(c) positive pulse width:

(d) duty cycle:

Question 4 — 2 marks

A synchronous digital logic circuit has a maximum propagation delay through any combinational logic path of 4 ns. The registers in this circuit have a clock-to-output delay of 0.5 ns and a minimum required setup time of 0.5 ns. What is the maximum clock rate at which this circuit will operate reliably?

Question 5 — 5 marks

A state machine has two inputs named **a** and **b**. Its state can be represented as a two-bit value. The state transition table for the state machine is shown below and follows the conventions used in the lecture notes.

Draw the state transition diagram for this state machine. Follow the conventions shown in the lecture notes for state transition diagrams. *Hint: Label the state transitions unambiguously.*

State	a	b	Next State
00	0	1	01
00	1	0	11
01	0	1	10
01	1	0	00
10	0	1	11
10	1	0	01
11	0	1	00
11	1	0	10

Question 6 — 2 marks

An IC has the following logic level specifications:

Table 5–5. 3.3-V LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.5	4.0	V
V_{IL}	Low-level input voltage		–0.5	0.65	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(1)*	2.6		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(1)*		0.35 V	

(a) What is the noise margin for a high logic level?

(b) What is the noise margin for a low logic level?

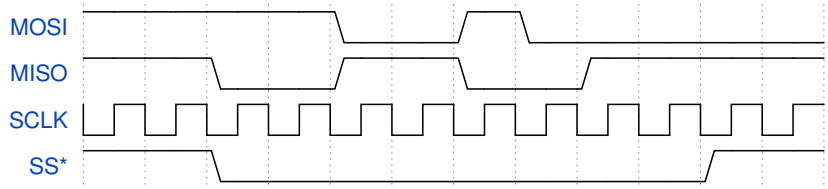
Question 7 — 2 marks

(a) What clock rate would be required to implement an 12-bit SAR ADC operating at a sampling rate of 64 kHz?

(b) The signal to noise ratio at the output of a DAC is 72 dB. The noise includes quantization noise and other effects such as distortion. What is the effective number of bits (ENOB)?

Question 8 — 3 marks

The waveforms below show a data transfer over an SPI interface. The interface follows the conventions described in the lecture notes.



(a) How many bits were transferred?

(b) What numerical value was transferred from the slave to the master? Give your answer as a hexadecimal number.

Question 9 — 2 marks

A digital circuit operating at 30 MHz consumes 100 mW. What clock rate would allow this circuit to operate for one year from a 3000 mW-h (milliwatt-hour) battery? *Hint: A year is approximately 3000 hours.*

Question 10 — 7 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

ready/valid	
ASIC	
FPGA	
feature size	
wafer	
NRE	
LE	

(1) interface

(2) used to manufacture die

(3) building block of a PLD

(4) measured in nanometers

(5) PLD

(6) one-time costs

(7) custom-designed IC

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This exam paper is for:

Sample Exam 2 A01234567

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Name: _____

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Signature: _____

Question 1 — 5 marks

Write a Verilog module named **`fastcount`** that has three one-bit inputs named **`clk`**, **`reset`**, and **`fast`**, and an 20-bit output named **`count`**.

`count` changes only on the rising edge of **`clk`**. If **`reset`** is asserted then **`count`** is set to 0. Otherwise **`count`** is incremented by 16 if **`fast`** is asserted, otherwise it is incremented by 1 .

Follow the course coding conventions but omit comments.

Question 2 — 5 marks

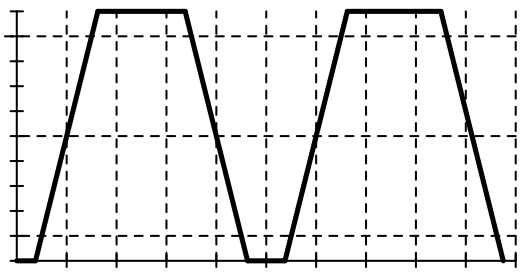
Fill in the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that **`x`** has the value **`8'hd6`** and that **`y`** has the value **`4'ha`**. The first row has been filled in as an example.

expression	value
`x[3:0]`	`4'h6`
`x[3:0] | y`	
`{ x[7:1], y>7 }`	
`x << y - 1`	
`{ ~y, 4'b1 }`	
`y >= 7 ? ! y : y + 1'b1`	

Question 3 — 4 marks



The diagram above shows an oscilloscope screen capture that includes one period of an *active-high* digital waveform. The scale on the horizontal axis is 25 ns per division. What are the values of the following? Include units and give your answers in nanoseconds or percent, as appropriate.

(a) rise time:

(b) period:

(c) positive pulse width:

(d) duty cycle:

Question 4 — 2 marks

A synchronous digital logic circuit has a maximum propagation delay through any combinational logic path of 10 ns. The registers in this circuit have a clock-to-output delay of 5 ns and a minimum required setup time of 5 ns. What is the maximum clock rate at which this circuit will operate reliably?

Question 5 — 5 marks

A state machine has two inputs named **a** and **b**. Its state can be represented as a two-bit value. The state transition table for the state machine is shown below and follows the conventions used in the lecture notes.

Draw the state transition diagram for this state machine. Follow the conventions shown in the lecture notes for state transition diagrams. *Hint: Label the state transitions unambiguously.*

State	a	b	Next State
00	0	1	01
00	1	0	00
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01	1	0	00
10	0	1	11
10	1	0	01
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V_{IL}	Low-level input voltage		–0.5	0.75	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(1)*	2.25		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(1)*		0.25	V

(a) What is the noise margin for a high logic level?

(b) What is the noise margin for a low logic level?

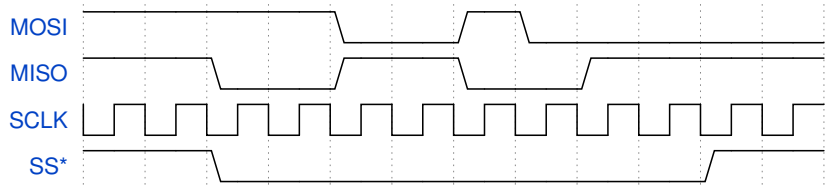
Question 7 — 2 marks

(a) What clock rate would be required to implement an 8-bit SAR ADC operating at a sampling rate of 64 kHz?

(b) The signal to noise ratio at the output of a DAC is 66 dB. The noise includes quantization noise and other effects such as distortion. What is the effective number of bits (ENOB)?

Question 8 — 3 marks

The waveforms below show a data transfer over an SPI interface. The interface follows the conventions described in the lecture notes.



(a) How many bits were transferred?

(b) What numerical value was transferred from the master to the slave? Give your answer as a hexadecimal number.

Question 9 — 2 marks

A digital circuit operating at 30 MHz consumes 200 mW. What clock rate would allow this circuit to operate for one year from a 3000 mW-h (milliwatt-hour) battery? *Hint: A year is approximately 3000 hours.*

Question 10 — 7 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

ready/valid	
ASIC	
FPGA	
feature size	
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(1) used to manufacture die

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