## Solutions to Quiz 3

## Question 1

The table(s) below shows part of the datasheet for a 74LS-series IC. What are the high- and low-level noise margins?

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

|  |  | Min | Max |  |
| :--- | :--- | :---: | :---: | :---: |
| VIH | Input HIGH Voltage | 2.0 |  | V |
| VIL | Input LOW Voltage |  | 0.8 | V |
| VOH | Output HIGH Voltage | 2.7 |  | V |
| VOL | Output LOW Voltage |  | 0.5 | V |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

|  |  | Min | Max |  |
| :--- | :--- | :---: | :---: | :---: |
| VIH | Input HIGH Voltage | 2.2 |  | V |
| VIL | Input LOW Voltage |  | 0.8 | V |
| VOH | Output HIGH Voltage | 2.7 |  | V |
| VOL | Output LOW Voltage |  | 0.4 | V |

## Answers

The high and low-level noise margins are (note the corrections to the $\mathrm{min} / \mathrm{max}$ notation for the equations in Lecture 7):

- noise margin(low) $=\mathrm{V}_{\mathrm{IL}(\text { max })}-\mathrm{V}_{\mathrm{OL}(\text { max })}$
- noise margin(high) $=\mathrm{V}_{\mathrm{OH}(\text { min })}-\mathrm{V}_{\mathrm{IH}(\text { min })}$

For the first example the high-level noise margin is $2.7-2.0=0.7 \mathrm{~V}$ and the low-level noise margin $0.8-0.5=0.3 \mathrm{~V}$.

For the first example the high-level noise margin is $2.7-2.2=0.5 \mathrm{~V}$ and the low-level noise margin $0.8-0.4=0.4 \mathrm{~V}$.

## Question 2

What logic function is implemented by the circuit on the right? Give your answer as a Boolean logic expression for Y involving $\mathrm{A}, \mathrm{B}$ and C .


## Answers

For the first circuit, if any of the transistors are turned on the output is pulled low. Thus the logic function is a 3-input NOR gate: $Y=\overline{\mathrm{A}+\mathrm{B}+\mathrm{C}}$.

For the second circuit, all of the transistors must be turned on for the output to be pulled low. Thus the logic function is a 3-input NAND gate: $Y=\overline{\mathrm{A} \cdot \mathrm{B} \cdot \mathrm{C}}$.

## Question 3

You are designing a circuit with an open-collector output. The rise-time time constant must be less than $100 \mu \mathrm{~s}$. The total capacitance to ground on this output is 35 (or 60 ) pF . What is the highest resistance that you can use for the pull-up resistor?

The time constant of the circuit is $\tau=R C$ and $C$ is given as 35 pF (or 60 pF ). To keep the time constant to less than $100 \mu \mathrm{~s}$ the resistance must be kept to less than $R=100 \mu \mathrm{~s} / 35 \mathrm{pF}=100 \times 10^{-6} / 35 \times 10^{-12} \approx 2.9 \mathrm{M} \Omega$ (or $1.7 \mathrm{M} \Omega)$.

