ELEX 2117 : Digital Techniques 2
2023 Winter Term

Quiz 2
1:30 – 2:20 PM
Friday, February 16, 2023
SW01-1021

This exam has two (2) questions on two (2) pages. The marks for each question are as indicated. There are a total of twenty-two (22) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

A signal (variable) has the value 1 in a Verilog statement. Would it be considered True or False?	
You need to set a one-bit output named $\overline{\texttt{first}}$ to a true value. Would you assign it a value of 0 or 1 in Verilog?	
An input indicates that something is ready when it is at a high logic level. Would this signal be named `ready` or $\overline{\texttt{ready}}$?	
An input named $\overline{\texttt{full}}$ indicates if something is full. If it is full, would the value read by a Verilog module have the value 0 or 1?	
The value read from an input port named `dark` is used in a Verilog expression and has a true value. Was that port at a high or low logic level?	

Question 2 — 17 marks

Label the underlined blanks in the diagram below and connect the module ports so the diagram matches the module `M`. There are two (2) missing module:instance names, ten (10) missing port names and five (5) missing connections. One module:instance name, two port names and two connections are shown as examples.

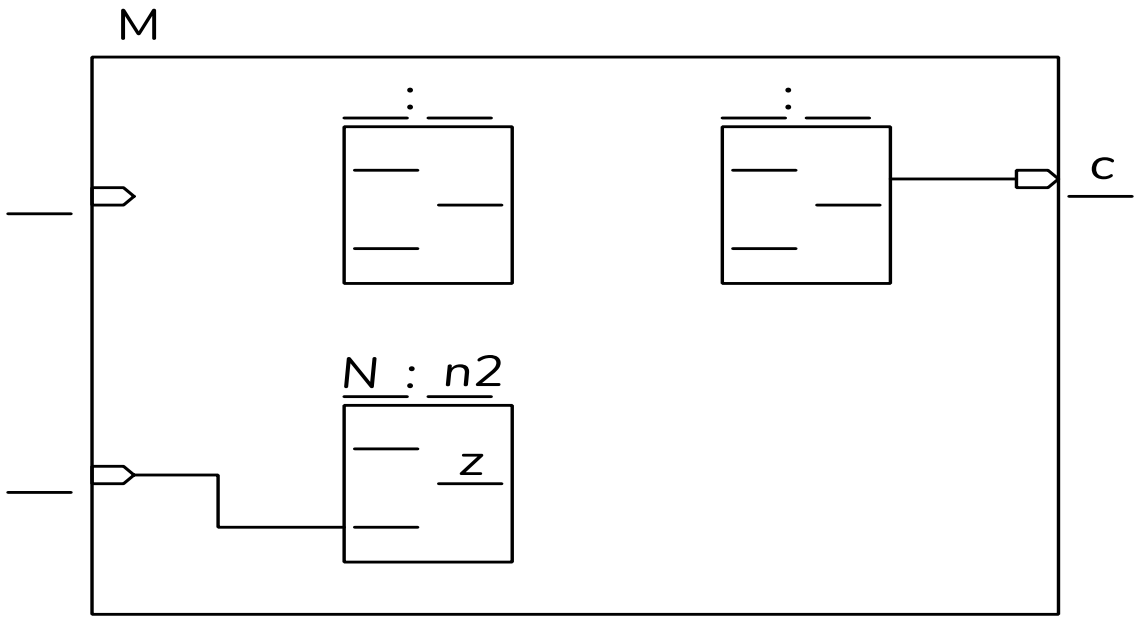
```
module N ( input logic x, y, output logic z ) ;
   // ...
endmodule
module O ( input logic a, b, output logic c ) ;
   // ...
endmodule

module M ( output logic c, input logic p1, p2 ) ;

   logic a, b ;

   N n1 (.z(a), .y(p1), .x(p2)) ;
   N n2 (p1, p2, b) ;
   O o1 (.*) ;

endmodule
```



ELEX 2117 : Digital Techniques 2

2023 Winter Term

Quiz 2

1:30 – 2:20 PM

Friday, February 16, 2023

SW01-1021

This exam has two (2) questions on two (2) pages. The marks for each question are as indicated. There are a total of twenty-two (22) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 2 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

A signal (variable) has the value 0 in a Verilog statement. Would it be considered True or False?	
You need to set a one-bit output named **`first`** to a true value. Would you assign it a value of 0 or 1 in Verilog?	
An input indicates that something is ready when it is at a low logic level. Would this signal be named **`ready`** or $\overline{\texttt{ready}}$?	
An input named **`full`** indicates if something is full. If it is full, would the value read by a Verilog module have the value 0 or 1?	
The value read from an input port named $\overline{\texttt{dark}}$ is used in a Verilog expression and has a true value. Was that port at a high or low logic level?	

Question 2 — 17 marks

Label the underlined blanks in the diagram below and connect the module ports so the diagram matches the module **`M`**. There are two (2) missing module:instance names, ten (10) missing port names and five (5) missing connections. One module:instance name, two port names and two connections are shown as examples.

```
module N ( input logic x, y, output logic z ) ;
   // ...
endmodule
module O ( input logic a, b, output logic c ) ;
   // ...
endmodule

module M ( output logic c, input logic p1, p2 ) ;

   logic a, b ;

   N n1 (.z(a), .y(p1), .x(p2)) ;
   N n2 (p1, p2, b) ;
   O o1 (.*) ;

endmodule
```