

Solutions to Quiz 1

There were two versions of each question. The values and the answers for both versions are given below.

Question 1

Write a Verilog module named q1 that has two logic inputs named v0 and v1 and two logic outputs named vor and vand (or vxor and vall). Leave the module empty – it should have no statements other than module and endmodule.

Answers

```
module q1
  ( input logic v0, v1,
    output logic vor, vand );
endmodule
```

```
module q1
  ( input logic v0, v1,
    output logic vxor, vall );
endmodule
```

expression	value
b[3:0]	4'h6
!a[0]	
{ a[2:1], 2'b11 }	
a + b == 0	
'1 ^ a	
a && !b	
a[0] ? 1 : 2	
b >> 2	

Question 2

Write a Verilog literal that has a width of 8 (or 4) bits, uses a hexadecimal (or decimal) base and has a value of 18 (or 12) (decimal).

Answers

8'h12 (or 4'd12).

Question 3

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] a ;
logic [3:0] b ;
```

and that a has the value 8'ha5 (or 8'h5a) and that b has the value 4'b0110. The first row has been filled in as an example.

Answers

For:

```
logic [7:0] a = 8'h5a ; // 0101_1010
logic [3:0] b = 4'b0110 ;
```

and

```
logic [7:0] a = 8'ha5 ; // 1010_0101
logic [3:0] b = 4'b0110 ;
```

the values are:

expression	value	value
b[3:0]	4'h6	4'h6
!a[0]	1'h1	1'h0
{a[2:1], 2'b11}	4'h7	4'hb
a + b == 0	1'h0	1'h0
'1 ^ a	8'ha5	8'h5a
a && !b	1'h0	1'h0
a[0] ? 1 : 2	32'h2	32'h1
b>>2	4'h1	4'h1

Question 4

Draw a block diagram (a schematic) that corresponds to the following Verilog module:

```
module x ( input  logic [7:0] a,  
           output logic [7:0] y ) ;  
    assign y = a > 2 ? a : a+1'b1 ;  
endmodule
```

or

```
module x ( input logic clk,  
           output logic [7:0] y ) ;  
    always_ff @(posedge clk)  
        y <= y + 1'b1 ;  
endmodule
```

Follow the guidelines in the Diagrams section of the Report and Video Guidelines document.

Answers

