ELEX 2117 : Digital Techniques 2
2023 Winter Term

Quiz 1
1:30 – 2:20 PM
Friday, January 20, 2023
SW01-1021

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of sixteen (16) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 3 marks

Write a Verilog module named `q1` that has two logic inputs named `v0` and `v1` and two logic outputs named `vxor` and `vall`. Leave the module empty – it should have no statements other than module and endmodule.

Question 2 — 2 marks

Write a Verilog literal that has a width of 4 bits, uses a decimal base and has a value of 12 (decimal).

Question 3 — 7 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] a ;
logic [3:0] b ;
```

and that `a` has the value `8'h5a` and that `b` has the value `4'b0110`. The first row has been filled in as an example.

expression	value
`b[3:0]`	`4'h6`
`!a[0]`	
`{ a[2:1], 2'b11 }`	
`a + b == 0`	
`'1 ^ a`	
`a && !b`	
`a[0] ? 1 : 2`	
`b >> 2`	

Question 4 — 4 marks

Draw a block diagram (a schematic) that corresponds to the following Verilog module:

```
module x ( input logic clk,
           output logic [7:0] y ) ;
   always_ff @(posedge clk)
     y <= y + 1'b1 ;
endmodule
```

Follow the guidelines in the Diagrams section of the Report and Video Guidelines document.

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Paper, Test 2 A00123456

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Name: _____

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Question 1 — 3 marks

Write a Verilog module named `q1` that has two logic inputs named `v0` and `v1` and two logic outputs named `vor` and `vand`. Leave the module empty – it should have no statements other than `module` and `endmodule`.

Question 2 — 2 marks

Write a Verilog literal that has a width of 8 bits, uses a hexadecimal base and has a value of 18 (decimal).

Question 3 — 7 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] a ;
logic [3:0] b ;
```

and that `a` has the value `8'ha5` and that `b` has the value `4'b0110`. The first row has been filled in as an example.

expression	value
`b[3:0]`	`4'h6`
`!a[0]`	
`{ a[2:1], 2'b11 }`	
`a + b == 0`	
`'1 ^ a`	
`a && !b`	
`a[0] ? 1 : 2`	
`b >> 2`	

Question 4 — 4 marks

Draw a block diagram (a schematic) that corresponds to the following Verilog module:

```
module x ( input  logic [7:0] a,
           output logic [7:0] y ) ;
  assign y = a > 2 ? a : a+1'b1 ;
endmodule
```

Follow the guidelines in the Diagrams section of the Report and Video Guidelines document.