ELEX 2117 : Digital Techniques 2
2023 Winter Term

MIDTERM EXAM 2
15:30 – 17:20
Friday, March 3, 2023
SW01-1205

This exam has six (6) questions on one (1) pages. The marks for each question are as indicated. There are a total of fourteen (14) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

Write a Verilog module named **pmark** that has a single-bit reset input named **reset**, a single-bit clock input named **clock** and a single-bit **logic** output named **mark**.

This module should implement two counters. If **reset** is asserted both counters should be set to zero on the next rising clock edge.

Otherwise, the first counter should continuously count down from 30 to zero and the second counter should continuously count down from 12 to zero. The two counters operate independently except when **reset** is asserted.

The **mark** output should be set high when both counters have a value of zero, and should be set low otherwise.

Question 2 — 2 marks

What are the period and duty cycle of the active-high **logic** signal **x** that is generated by the following Verilog in a testbench:

```
always begin
   #20ns x = 1'b0 ;
   #10ns x = 1'b1 ;
end
```

Question 3 — 2 marks

Write System Verilog code that could be included in a testbench to print the value of the logic signal **x** each time the value of the signal **y** changes. The code that changes **y** is not given. You may use any System Verilog language features and you may print the value of **x** in any format.

Question 4 — 2 marks

You wish to ensure a logic circuit will operate reliably. What is the maximum allowed propagation delay through any combinational logic path if the clock rate is 100 MHz, the registers have a 3 ns setup time, and a 2 ns clock-to-output delay? Show your work.

Question 5 — 1 marks

A signal is low when a motor is running. Would you name this signal **run** or $\overline{\texttt{run}}$?

Question 6 — 2 marks

Is a propagation delay a timing requirement or a guaranteed response? Why?

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This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

Write a Verilog module named **`xmark`** that has a single-bit reset input named **`reset`**, a single-bit clock input named **`clock`** and a single-bit **`logic`** output named **`mark`**.

This module should implement two counters. If **`reset`** is asserted both counters should be set to zero on the next rising clock edge.

Otherwise, the first counter should continuously count down from 30 to zero and the second counter should continuously count down from 12 to zero. The two counters operate independently except when **`reset`** is asserted.

The **`mark`** output should be set high when both counters have a value of zero, and should be set low otherwise.

Question 2 — 2 marks

What are the period and duty cycle of the active-high **`logic`** signal **`x`** that is generated by the following Verilog in a testbench:

```
always begin
   #10ns x = 1'b0 ;
   #20ns x = 1'b1 ;
end
```

Question 3 — 2 marks

Write System Verilog code that could be included in a testbench to print the value of the logic signal **`x`** each time the value of the signal **`y`** changes. The code that changes **`y`** is not given. You may use any System Verilog language features and you may print the value of **`x`** in any format.

Question 4 — 2 marks

You wish to ensure a logic circuit will operate reliably. What is the maximum allowed propagation delay through any combinational logic path if the clock rate is 10 MHz, the registers have a 30 ns setup time, and a 20 ns clock-to-output delay? Show your work.

Question 5 — 1 marks

A signal is high when a motor is running. Would you name this signal **`run`** or $\overline{\texttt{run}}$?

Question 6 — 2 marks

Is the period of a clock input a timing requirement or a guaranteed response? Why?