Solutions to Midterm 1

There were two versions of each question. The answers for both versions are given below.

Question 1

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] a ;
logic [3:0] b ;
```

and that `a` has the value `8'ha5` (or `8'h33`) and that `b` has the value `4'b0110` (or `4'b1001`). The first row has been filled in as an example.

expression	value
`a[3:0]`	`4'h5`
`a+8'b1`	
`{a[3:0],2'b2}`	
`b<<(b!=0)`	
`~b[0]?b[1]:(b[2]?b[3]:4)`	

Answers

For `a=8'ha5` and `b=4'b0110`, the results are:

expression	value
`a[3:0]`	`4'h5`
`a+8'b1`	`8'ha6`
`{a[3:0],2'd2}`	`6'h16`
`b<<(b!=0)`	`4'hc`
`~b[0]?b[1]:(b[2]?b[3]:4)`	`32'h1`

For `a=8'h33` and `b=4'b1001`, the results are:

a[3:0]	4'h3
a+8'b1	8'h34
{a[3:0],2'd2}	6'he
b<<(b!=0)	4'h2
~b[0]?b[1]:(b[2]?b[3]:4)	32'h4

Question 2

A counter is used to implement a delay of 5 (or 10) milliseconds. The clock used to decrement the counter has a frequency of 20 (or 10) MHz. If the counter counts down to zero, what initial value should be loaded into the counter? Show your work.

Answers

N clock periods of duration $T = 1/f$ where f is the clock frequency results in a total duration of $N/T = Nf$. If the counter counts down to zero the initial count value should be $N-1$. For $T = 5$ ms and $f = 20$ MHz the initial count value should be $5\times10^{-3}\times 20\times10^{6}-1 = 100\times10^{3}-1 = \boxed{99,999}$. For $T = 10$ ms and $f = 10$ MHz the initial count value should be $10\times10^{-3}\times10\times10^{6}-1 = 100\times10^{3}-1 = \boxed{99,999}$.

Question 3

A state machine has three 1-bit inputs named `r`, `s`, and `t`; and a 2-bit output named `out` that is also the state. `out` can take on the binary values `11` (or `00`), `01`, and `10`. The state machine operates as follows:

- If `out` is any value and `r` is asserted (has the value 1) then `out` is set to `11` (or `00`).
- If `out` is `11` (or `00`) and `s` is asserted then `out` is set to `10`.
- If `out` is `10` and `t` is asserted then `out` is set to `01`.

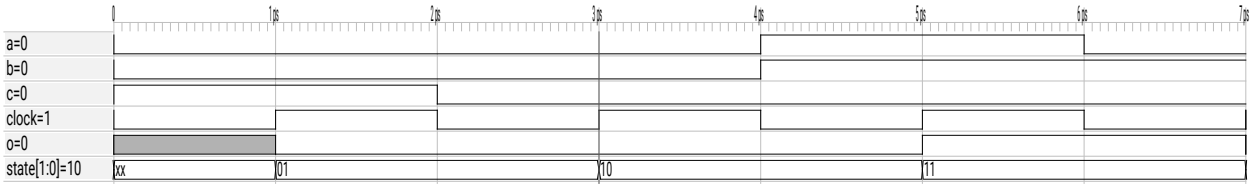


Figure 1: Question 5 Simulation Results

- If **out** is **01** and **t** is asserted then **out** is set to **10**.
- In all other cases the state does not change.

Write a state transition table for this state machine. Include columns for the current state, the **r**,**s**, and **t** inputs and the next state. *Hint: use* ***X*** *as don't care*

Answers

out	r	s	t	next out
X	1	X	X	11
11	0	1	X	10
10	0	X	1	01
01	0	X	1	10

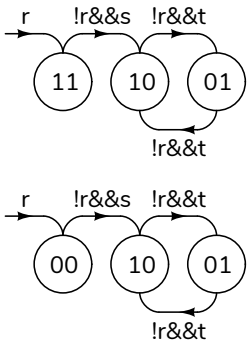
or

out	r	s	t	next out
X	1	X	X	00
00	0	1	X	10
10	0	X	1	01
01	0	X	1	10

Question 4

Draw the state transition diagram for the state machine described in the previous question. Follow the course guidelines.

Answers



Question 5

Write a System Verilog module named **midterm** that implements a state machine with the following state transition table:

State	inputs			Next State
	a	b	c	
X	X	X	1	2'd1
2'd1	X	X	0	2'd2
2'd2	1	1	X	2'd3
2'd3	0	1	X	2'd2

Conditions that are not listed do not result in a change of state.

The module should have three 1-bit input signals named **a**, **b**, and **c**; a 1-bit output named **o**; and an input clock signal named **clock**. The output **o** is only asserted in state **2'd3** (or **2'd2**). Follow the course coding guidelines.

Answers

The course guidelines state that the first matching condition in the table has priority. This means the first row (reset) takes priority over other rows when **c** is asserted.

```
module midterm
  ( input logic a, b, c,
    output logic o,
    input logic clock ) ;

   logic [1:0] state ;

   always_ff @(posedge clock) state
     <=                          c ? 2'd1 :
        state == 2'd1 &&        !c ? 2'd2 :
        state == 2'd2 &&  a && b ? 2'd3 :
        state == 2'd3 && !a && b ? 2'd2 : state ;

   assign o = state == 2'd3 ; // or state == 2'd2

endmodule
```

A simulation result showing each transition is in Figure 1.