ELEX 2117 : Digital Techniques 2
2023 Winter Term

MIDTERM EXAM 1
15:30 – 17:20
Friday, February 3, 2023
SW01-1205

This exam has five (5) questions on two (2) pages. The marks for each question are as indicated. There are a total of twenty-two (22) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 4 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] a ;
logic [3:0] b ;
```

and that `a` has the value `8'h33` and that `b` has the value `4'b1001`. The first row has been filled in as an example.

expression	value
a[3:0]	4'h5
a+8'b1	
{a[3:0],2'b2}	
b<<(b!=0)	
~b[0]?b[1]:(b[2]?b[3]:4)	

Question 2 — 2 marks

A counter is used to implement a delay of 10 milliseconds. The clock used to decrement the counter has a frequency of 10 MHz. If the counter counts down to zero, what initial value should be loaded into the counter? Show your work.

Question 3 — 4 marks

A state machine has three 1-bit inputs named `r`, `s`, and `t`; and a 2-bit output named `out` that is also the state. `out` can take on the binary values `00`, `01`, and `10`. The state machine operates as follows:

- If `out` is any value and `r` is asserted (has the value 1) then `out` is set to `00`.
- If `out` is `00` and `s` is asserted then `out` is set to `10`.
- If `out` is `10` and `t` is asserted then `out` is set to `01`.
- If `out` is `01` and `t` is asserted then `out` is set to `10`.
- In all other cases the state does not change.

Write a state transition table for this state machine. Include columns for the current state, the `r`,`s`, and `t` inputs and the next state. *Hint: use `X` as don't care*

Question 4 — 5 marks

Draw the state transition diagram for the state machine described in the previous question. Follow the course guidelines.

Question 5 — 7 marks

Write a System Verilog module named **`midterm`** that implements a state machine with the following state transition table:

State	inputs			Next State
	a	b	c	
X	X	X	1	2'd1
2'd1	X	X	0	2'd2
2'd2	1	1	X	2'd3
2'd3	0	1	X	2'd2

Conditions that are not listed do not result in a change of state.

The module should have three 1-bit input signals named **`a`**, **`b`**, and **`c`**; a 1-bit output named **`o`**; and an input clock signal named **`clock`**. The output **`o`** is only asserted in state **`2'd2`**. Follow the course coding guidelines.

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This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 4 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in hexadecimal base. Assume the following declarations:

```
logic [7:0] a ;
logic [3:0] b ;
```

and that `a` has the value `8'ha5` and that `b` has the value `4'b0110`. The first row has been filled in as an example.

expression	value
a[3:0]	4'h5
a+8'b1	
{a[3:0],2'b2}	
b<<(b!=0)	
~b[0]?b[1]:(b[2]?b[3]:4)	

Question 2 — 2 marks

A counter is used to implement a delay of 5 milliseconds. The clock used to decrement the counter has a frequency of 20 MHz. If the counter counts down to zero, what initial value should be loaded into the counter? Show your work.

Question 3 — 4 marks

A state machine has three 1-bit inputs named `r`, `s`, and `t`; and a 2-bit output named `out` that is also the state. `out` can take on the binary values `11`, `01`, and `10`. The state machine operates as follows:

- If `out` is any value and `r` is asserted (has the value 1) then `out` is set to `11`.
- If `out` is `11` and `s` is asserted then `out` is set to `10`.
- If `out` is `10` and `t` is asserted then `out` is set to `01`.
- If `out` is `01` and `t` is asserted then `out` is set to `10`.
- In all other cases the state does not change.

Write a state transition table for this state machine. Include columns for the current state, the `r`,`s`, and `t` inputs and the next state. *Hint: use `X` as don't care*

Question 4 — 5 marks

Draw the state transition diagram for the state machine described in the previous question. Follow the course guidelines.

Question 5 — 7 marks

Write a System Verilog module named **`midterm`** that implements a state machine with the following state transition table:

State	inputs			Next State
	a	b	c	
X	X	X	1	2'd1
2'd1	X	X	0	2'd2
2'd2	1	1	X	2'd3
2'd3	0	1	X	2'd2

Conditions that are not listed do not result in a change of state.

The module should have three 1-bit input signals named **`a`**, **`b`**, and **`c`**; a 1-bit output named **`o`**; and an input clock signal named **`clock`**. The output **`o`** is only asserted in state **`2'd3`**. Follow the course coding guidelines.