Programmable Logic Applications and Architectures

Exercise 1: Would you use hardware or software to implement: A new calculator? A digital watch? A controller for a kitchen appliance? An Ethernet interface? For Cryptocurrency "mining"? For an aircraft's automated landing system?

calculator - s/w

watch - h/w

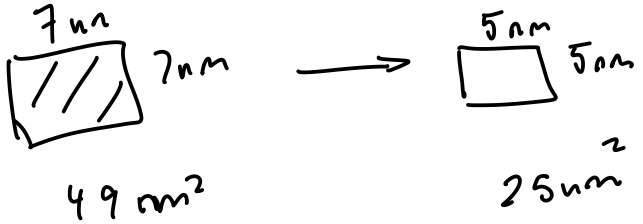
kitchen appliance - s/w

Ethernet - h/w

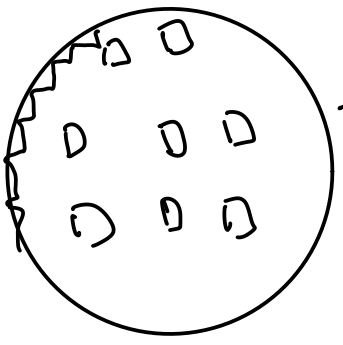
Crypto mining - h/w

landing system - either < special s/w dev / h/w

Exercise 2: What improvement in number of transistors per unit area would be achieved by reducing the ~~transistor~~ feature dimensions from 7 nm to 5 nm? Approximately how many 5x5 mm die fit on a 300 mm wafer? How many 200x200 nm gates fit on the die?



$49\,nm^2$ $25nm^2$ — approx. double



$$area = \pi r^2$$

$$die = \frac{\pi \cdot 150\,mm^2}{5nm^2} \approx 2700$$

$$gates = \left(\frac{5 \times 10^{-3}}{0.2 \times 10^{-6}}\right)^2 = (25 \times 10^3)^2 = 625 \times 10^6$$

Exercise 3: Would you use a PLD or ASIC for: A project that had to be completed within a month? That would be expected to sell 100 million units? Whose complete requirements aren't known? A state-of-the-art general-purpose CPU?

- 1 month TTM ? → PLD
- large volumes. → ASIC
- uncertain reqmnts → PLD
- competitive perf. → ASIC