Analog Interfaces

Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one that demonstrates aliasing and one that does not. Is it sufficient to sample at twice the highest frequency of the analog signal?

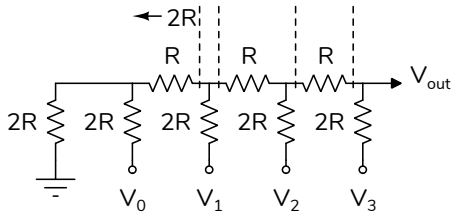
Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to include frequency components up to the 7'th harmonic (at 70 kHz)?

Exercise 3: A signal with range of ± 3 V must be quantized so that the quantization error is less than 1 mV. What minimum number of bits of resolution is required?

Exercise 4: A signal-to-noise power ratio of about 48 dB is considered good enough for speech communication. Approximately how many bits per sample are required to obtain this quantization SNR?

Exercise 5: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

Exercise 6:



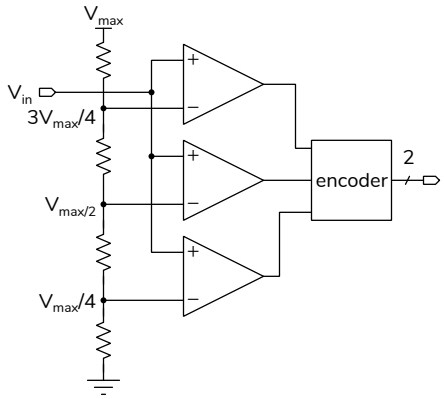
Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenim resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{\text{ref}}$).

Exercise 7: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?

Exercise 8: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?

Exercise 9: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

Exercise 10:



Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

Exercise 11: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output?

Exercise 12: What is the slope of an integrator, in $\mathrm{V/s}$, when charging a 100 nF capacitor with 5 V through a $100\,\mathrm{k\Omega}$ resistor?

Exercise 13: Rank the different ADCs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.