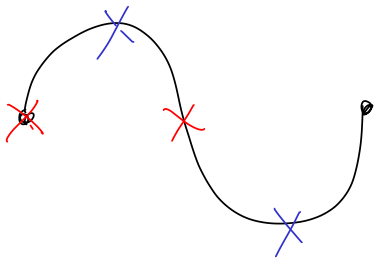
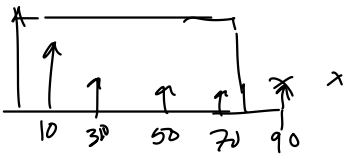
Analog Interfaces

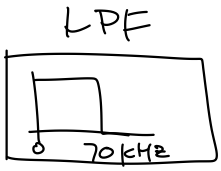
Exercise 1: Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one that demonstrates aliasing and one that does not. Is it sufficient to sample at twice the highest frequency of the analog signal?



No. $f_s > 2f_{max}$

Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to include frequency components up to the 7'th harmonic (at 70 kHz)?

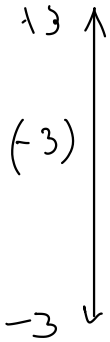




$f_s > 2 f_{max} = 2 \cdot 70\,kHz = 140\,kHz$

most sample at $> 140\,kHz$

Exercise 3: A signal with range of ±3 V must be quantized so that the quantization error is less than 1 mV. What minimum number of bits of resolution is required?



$V = 6V = 3 - (-3)$

$$\frac{V}{2^n - 1} = 1mV \qquad 2^n = \frac{6\,V}{1\,mV}$$

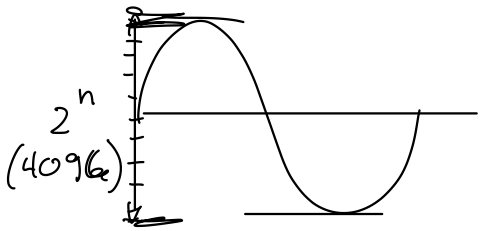
$$n = \log_2\left(\frac{6}{.001}\right) = \log_2(6000) = 12.5$$

use 13 bit resolution ADC.

Exercise 4: A signal-to-noise power ratio of about 48 dB is considered good enough for speech communication. Approximately how many bits per sample are required to obtain this quantization SNR?

$48 = 6B \qquad B = \frac{48}{6} = 8$ bits are needed

Exercise 5: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?



$n = 12$ bits

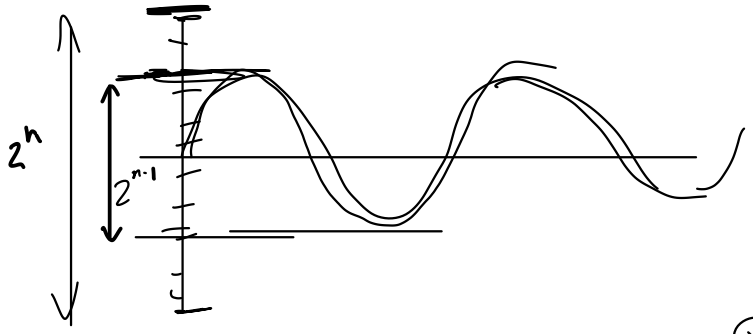
quantization SNR $= 1.76 + 6n$ dB

$= 1.76 + 6 \cdot 12$

≈ 74 dB

$74\,dB = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) = 10\log\left(\frac{V_{sig}}{V_{noise}}\right)^2$

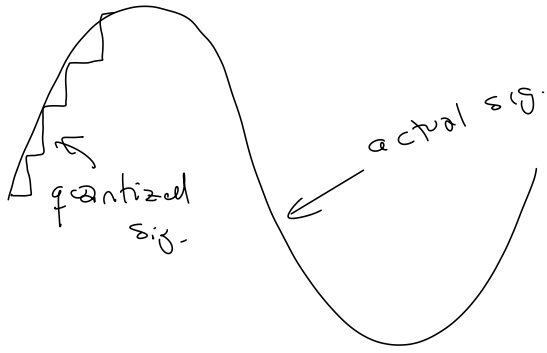
$= 20\log\left(\frac{V_{sig}}{V_{noise}}\right)$



equivalent to using

$n = 11$ bits of resolution

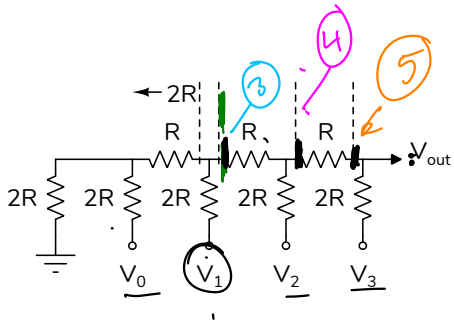
Quant. SNR $\approx 2 + 6 \cdot 11 = 68$ dB



$\text{SNR} = \frac{\text{signal power}}{\text{quant. noise power}}$

 ← quantization noise

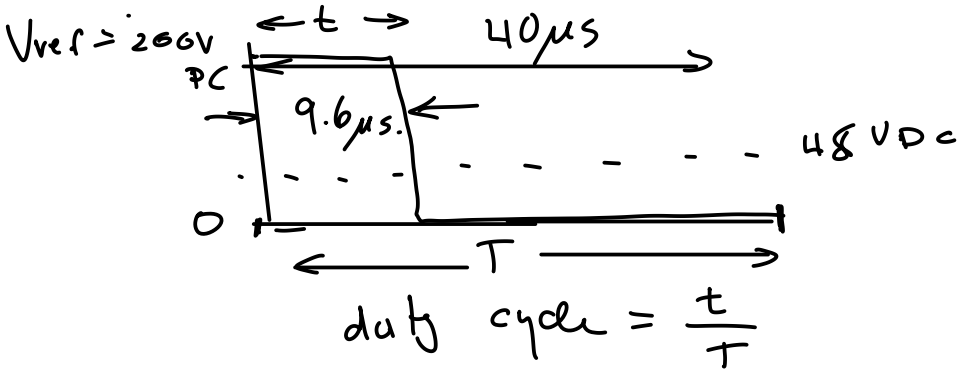
Exercise 6:



Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the Thevenim resistance (resistance to ground at V_{out} with all V_i shorted) and voltage (V_{out} with $V_1 = V_{ref}$).

Exercise 7: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The switching frequency is 25 kHz. What is the duration of each PWM pulse?

frequency → $\frac{1}{T}$



duty cycle = $\frac{t}{T}$

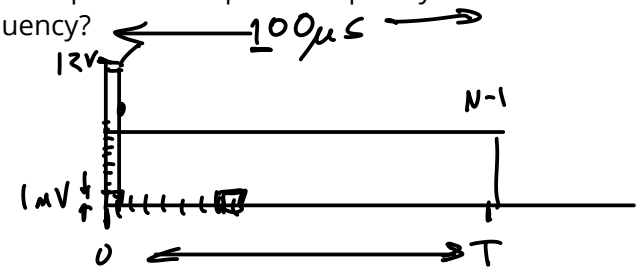
$V_{out} = \frac{t}{T} V_{ref}$

$t = \frac{V_{out}}{V_{ref}} \cdot T$

$= \frac{48}{200} \cdot \frac{1}{25 \times 10^3}$

$= 9.6\mu s.$

Exercise 8: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?



$t = \frac{1mV}{12V} \cdot T$

1mV ⇒ 1

12 V ⇒ N-1

$N \approx \frac{12}{1mV} \approx 12000$

$N = \log_2(12000)$ so we can count from 0 to 12000.

$= 14$ bits

$2^{10} = 1024$

$2^4 = 16$

$2^{14} = 16K$

$2^{13} = 8K$

t for minimum pulse duration

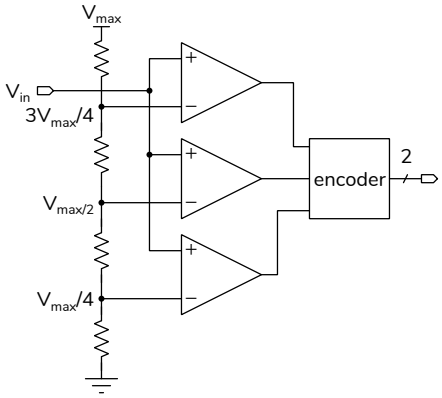
$= \frac{1}{12000} \cdot \frac{1}{10KHz}$

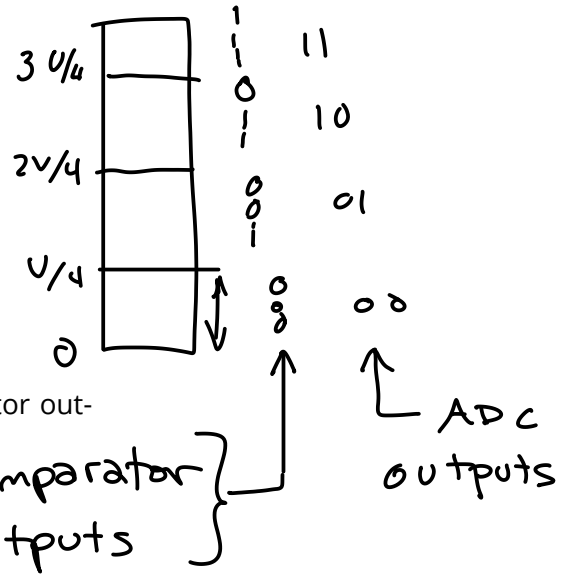
$freq = 12 \times 10^3 \cdot 10 \times 10^3 = 120\,MHz$

Exercise 9: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

	f_s / f_{clock} or bandwidth	complexity
– binary weighted DAC (e.g. R-2R)	1	2 resistors / bit need accurate resistors
– PWM	$\frac{1}{2^n - 1}$	grows as n
– Σ-Δ	$> \frac{1}{2^n - 1}$	grows as n

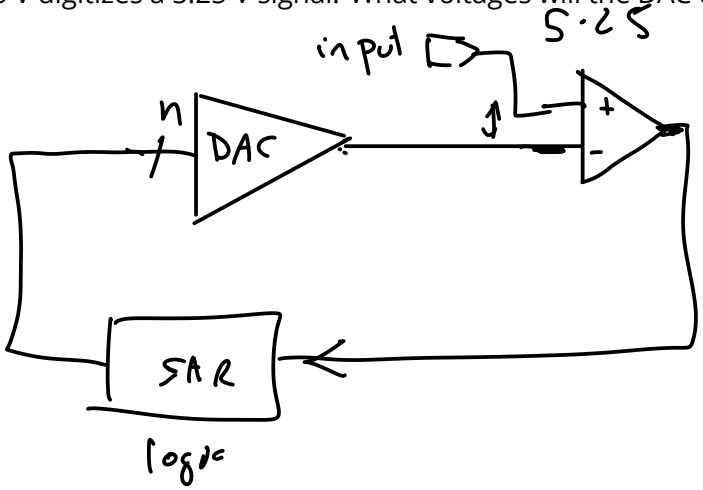
Exercise 10:

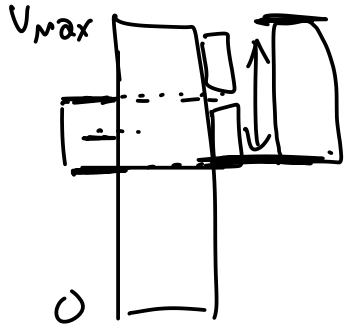


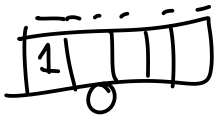


Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

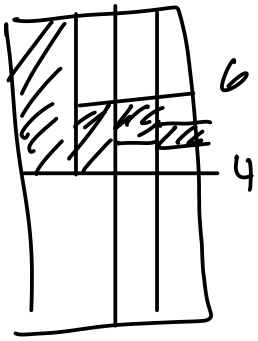
Exercise 11: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output?







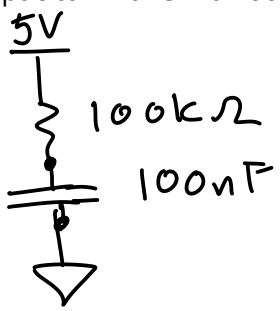
0 - 7.5	ref. V	comp. o/p
1000	→ 4.0 V	H
1100	→ 6.0 V	L
1010	→ 5.0 V	H
1011	→ 5.5 V	L
1010 ← final		

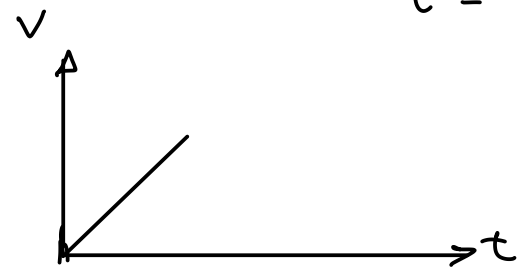


0	0000
0.5	0001
1.0	0010
1.5	0011
2.0	0100
2.5	0101
3.0	0110
3.5	0111
4.0	1000
4.5	1001
5.0	1010
5.5	1011
6.0	1100
6.5	1101
7.0	1110
7.5	1111

Exercise 12: What is the slope of an integrator, in V/s, when charging a 100 nF capacitor with 5 V through a 100 kΩ resistor?

$$i = C\frac{dV}{dt}$$





$$i(t=0) = \frac{5V}{100k} = 50\mu A = C\frac{dV}{dt}$$

$$\frac{dV}{dt} = \frac{i}{C} = \frac{50\times10^{-6}}{100\times10^{-9}} = 0.5\times10^{3} \left(500\,V/s.\right)$$

DACs
binary

Exercise 13: Rank the different ADCs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

	f_s/f_{clock}	complexity / resolution
flash	1	$O(2^n)$
SAR	f_s/n	$O(n)$ + 1 comp
ΣΔ	100 - 1000	O (1) + 1 comp
dual-slope	"	"
ramp.	"	"

PWM
ΣΔ

faster ↑ ↓ cheaper

high
low
accuracy

$O(n)$ means increases proportional to n.