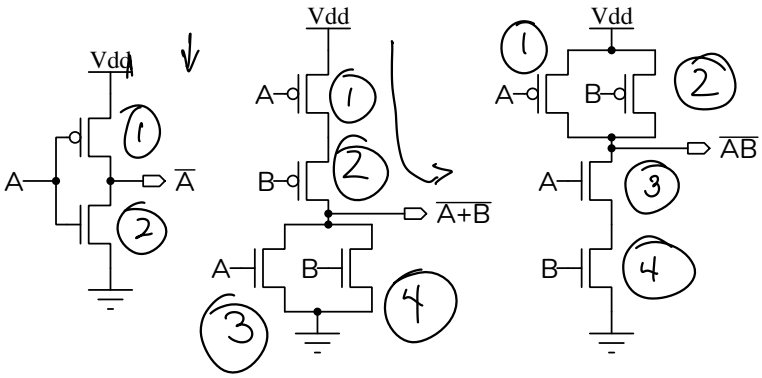
Implementation of Digital Logic Circuits

Exercise 1:



Which transistors are on when the output is high? When it is low?
In which direction does the output current flow in each case?

NOT

output:	H	L
ON:	1	2
OFF:	2	1

NOR

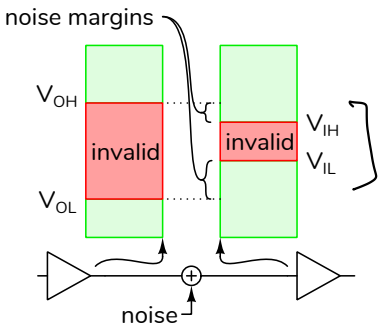
	H	L
	1 and 2	3 or 4
	3 and 4	1 or 2

NAND

	H	L
	1 or 2	3 and 4
	3 or 4	1 and 2

current flows in when output is low,
flows out when output is high.

Exercise 2:

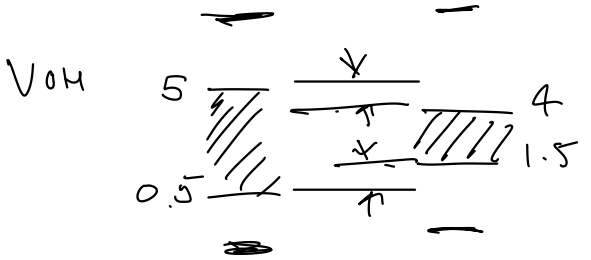


V_{IH}, V_{IL} } requirements.

V_{OH}, V_{OL} } guaranteed.

Which of these specifications does the manufacturer guarantee?
Which are requirements?

Exercise 3: A logic family has V_{OH}(min) = 5 V, V_{OL}(max) = 0.5 V, V_{IH}(min) = 4 V and V_{IL}(max) = 1.5 V. What are the noise margins?



high level noise margin = $5 - 4 = 1$ V

low level noise margin = $1.5 - 0.5 = 1$ V

Exercise 4: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

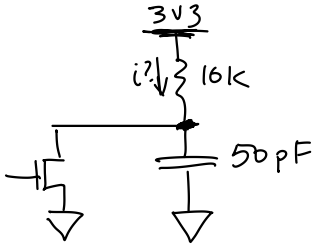
$$\frac{P_2}{P_1} = \left(\frac{V_2}{V_1}\right)^2 = \left(\frac{3.3}{5}\right)^2 \approx 0.44$$

reduction $= 1 - 0.44 = 56\%$

$$\frac{P_2}{P_1} = \left(\frac{1}{50}\right) = 0.02$$

reduction $= 1 - 0.02 = 98\%$

Exercise 5: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?

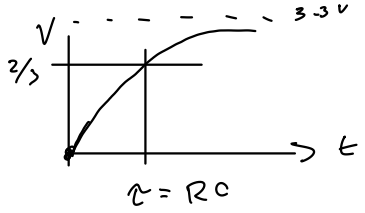


$$i = \frac{V}{R} = \frac{3.3 - 0}{10k} = 0.3\ mA$$

$$RC = 10 \times 10^3 \cdot 50 \times 10^{-12}\ s.$$

$$= 500 \times 10^{-9}\ s$$

$$= 0.5\ \mu s$$



Exercise 6: How many square mm of PCB area does each package require? Which packages have their pins accessible when the package is placed on the PCB?

484 mm^2

12 mm^2

TQFP has accessible pins (BGAs are under the package).