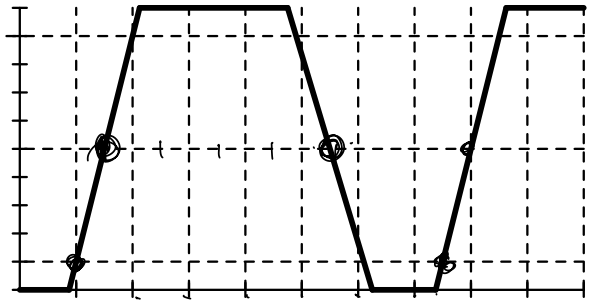
Timing Analysis

Exercise 1:



The diagram above shows an oscilloscope screen capture that includes one period of an active-low digital waveform. The scale on the horizontal axis is 20 ns per division. What are: the rise time, period, positive pulse width and duty cycle?

rise time = 1 div. = 20 ns.

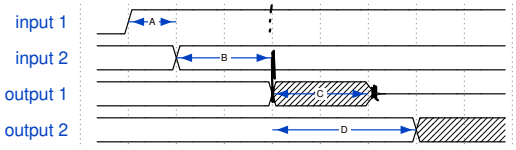
period = 6.5 div = 6.5 x 20 = 130 ns.

+ve pulse width = 4 div = 4 · 20 = 80 ns.

-ve pulse width = 2.5 div. = 2.5 x 20 = 50 ns.

$$\text{duty cycle} = \frac{50}{130} \approx 38\%$$

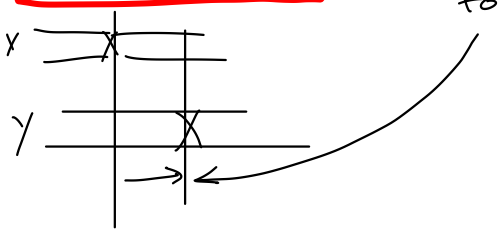
Exercise 2:



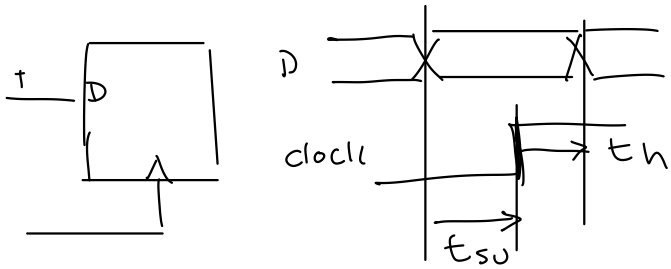
A is req.
B is guar.
C is guar.
D is guaranteed resp.

Label the specifications A through D as requirements or guaranteed responses. Which specifications are measured to a signal being in a high-impedance state? Which are measured from a rising edge only? From either?

Exercise 3: Is t_{PD} a requirement or a guaranteed response? ← because it's measured to an output



Exercise 4: Is t_{SU} a requirement or a guaranteed response? How about t_H?



t_{SU} is a requirement

t_H is a requirement

} both measurements end on inputs (clock & D respectively)

Exercise 5:

$$t_{SU}\text{ (avail)} = T_{clock} - t_{CO}\text{ (max)} - t_{PD}\text{ (max)}$$

Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

t_{CO} & t_{PD} decrease t_{su}(avail)

T_{clock} increase t_{su} (avail)

Exercise 6: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

$$t_{su(avail)} = T_{clock} - t_{co(max)} - t_{PD(max)}$$

$$T_{clock} = \frac{1}{f_{clock}} = \frac{1}{50 \times 10^6} = 20 ns.$$

$t_{co} = 2 ns \quad t_{PD} = 15 ns$

$t_{su} = 20 - 2 - 15 = 3 ns.$

slack = $3 - 5 = -2$

$t_{su(avail} - t_{su(req)} =$

need to add 2ns to T_{clock}

new $T_{clock} = 20 + 2 = 22 ns.$

new $f_{clock} = \frac{1}{22 \times 10^{-9}} = 45.5 MHz$

Exercise 7: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps hold times and adder logic that has a 250 ps propagation delay? ~~t_{co}~~

$t_{su} = 200\ ps$ (req'd)

$t_h = 50ps$ (max)

$t_{PD} = 250ps$ (max)

$t_{su(avail)} = T_{clock} - t_{co(max)} - t_{PD(max)}$

maximum clock frequency is for slack = 0,

i.e. $t_{su(avail)} = t_{su(req'd)}$

$T_{clock(min)} = t_{su(req'd)} + t_{co(max)} + t_{PD(max)}$

$= 200 + 50 + 250$

$= 500\ ps$

$f_{clock(max)} = \frac{1}{0.5 \times 10^{-9}} = 2\ GHz$