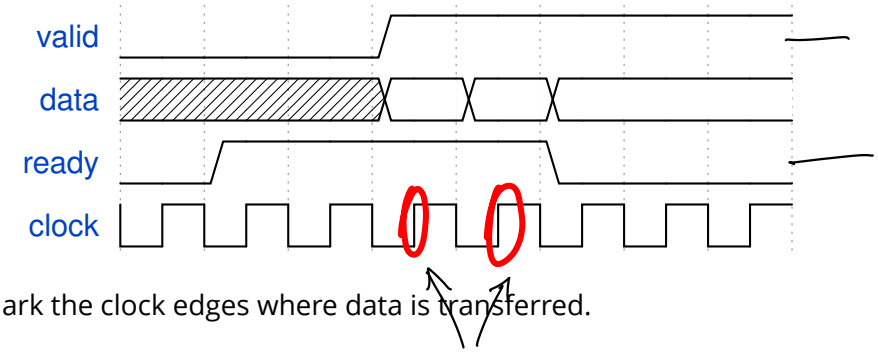
Interfaces

Exercise 1:

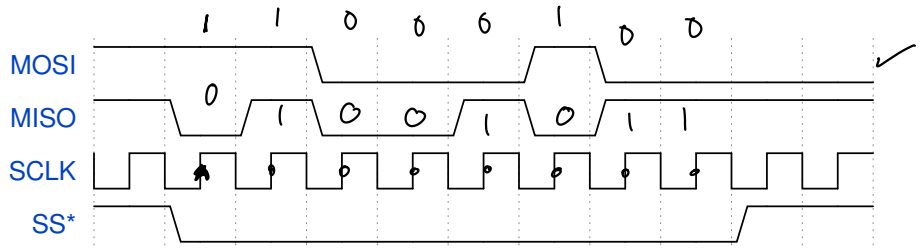


Mark the clock edges where data is transferred.

here:

when both valid and ready are asserted

Exercise 2:



The diagram above shows a transfer over an SPI bus. How many bits of data are transferred? What is the value, in decimal, of the data transferred from the master to the slave? From the slave to the master?

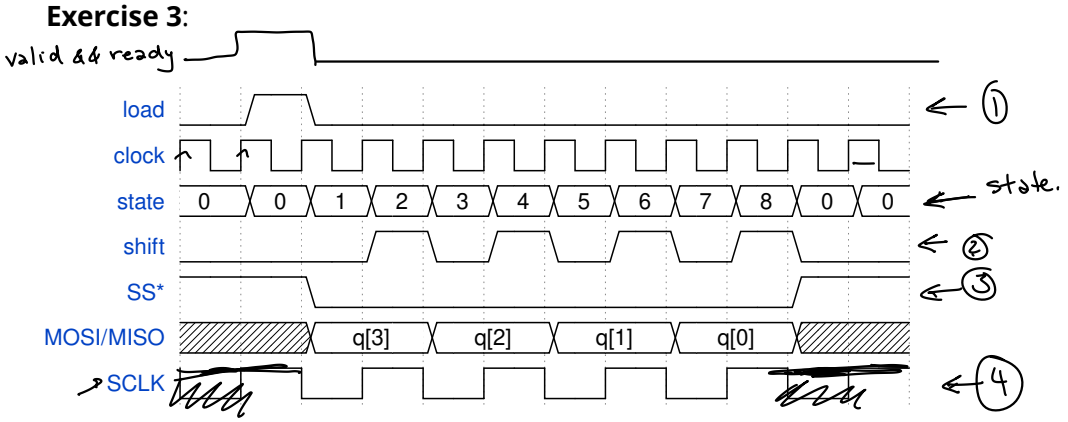
- 8 bits (rising clock edges while $\overline{SS}$ is asserted).
- from master to slave (MOSI):

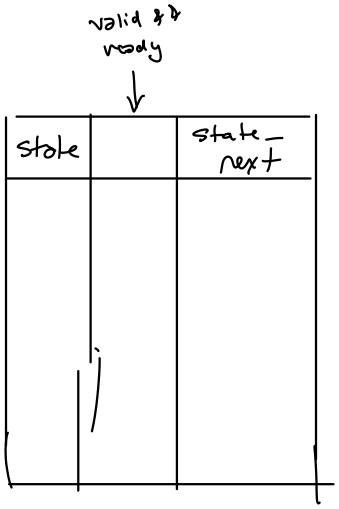
1 1 0 0 0 1 0 0 $\quad 8'hC4 = 196_{10}$

- from slave to master (MISO)

0 1 0 0 1 0 1 1 $\quad 8'h4b = 8'd75$

Exercise 3:





Based on the diagram above, write a state transition table for an SPI interface controller that transfers four bits at a time. Include an idle state. In which states are **SCLK** and **$\overline{\text{SS}}$** asserted?

sclk is asserted in states 0, 2, 4 ... 8

```
assign  sclk = !state[0];
assign  ss_n = state == 0;
assign  shift = state == 2 || state == 4
                || state == 6 || state == 8;
assign  load = valid && ready;

assign  state_next =
          !state && valid && ready ? 1 :   (C)
          !state ? 0 :                     (B)
          state == 8 ? 0 :                 (D)
          state ? state + 1 : state;       (A)
```

state transition diagram: