

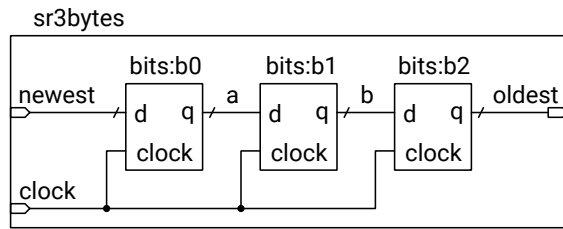
More Verilog

Exercise 1: Is a signal named $\overline{\text{overload}}$ active-high or active-low? Is there an overload if this signal is high? What if the signal was named **overload**?

Exercise 2: Come up with active-high and an active-low names for a signal that is at 3 V when a door is open and 0 V when the door is closed.

Exercise 3: If \bar{D} is a word and $\overline{D[\emptyset]}$ is low, is the word an even or odd number?

Exercise 4:



Draw a diagram for this instantiation of the `bits` module. Label the module, instance, signal and port names as in the diagram above.

Exercise 5:

```
module sr3bytes
(
  input logic [7:0] newest,
  output logic [7:0] oldest,
  input logic clock
) ;

localparam nbits = 8 ;

logic [nbits-1:0] a, b ;

// matching by order
bits #(nbits) b0 (newest,a,clock);

// matching by name (order does not matter)
bits #(.nb(nbits)) b1 (.q(b),.clock,.d(a));

// wildcards for names that match
bits #(.nb(nbits)) b2 (.d(b),.q(oldest),.*);

endmodule
```

Identify the module instantiation statements in the code above. For each one, what is the instantiated module's name? The instance name?

Exercise 6: What are the values of the following expressions: `|4' b0001,`
`^4' b1001, &4' b1111, &4' b1110?`

Exercise 7:

```
// concatenation:  
logic [3:0] x = { 2'b00, 2'b11 } ;  
  
// replication (z=8'b1010_1010):  
logic [7:0] y = { 4{2'b10} } ;  
  
// array literal  
logic [0:1] [3:0] z = '{ 4'b0011, 4'b1010 } ;
```

What are the dimensions and initial values of x, y, and z in the examples above?