

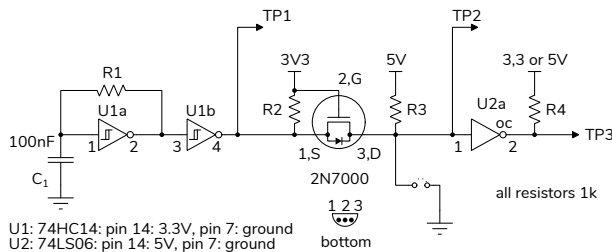
Logic Level Conversion

Revision 2 - screen capture 3 should include TP1 and TP3 (not TP1 and TP2 as in the Report section).

Introduction

In this lab you will build an oscillator, two logic-level converters, and make measurements using an oscilloscope.

The following schematic shows the circuit you will be measuring at the test points TP1, TP2 and TP3:



Voltages used in logic circuits are a compromise between power consumption and noise immunity. ICs made with bipolar transistors typically use 5 V logic levels. ICs made with CMOS transistors often use 3.3 V IO logic levels. When both types of devices are used in the same circuit it's necessary to convert between different logic levels.

The lecture notes describe simple techniques, such as voltage dividers, diode clamps and MOSFET switches to convert between logic levels. In this lab you will build and test the two logic level conversion circuits shown in the schematic above.

U1, a 74HC14 hex Schmidt trigger inverter, uses CMOS gates with a supply voltage of 3.3 V and logic levels of 0 and 3.3 V.

U2, a 74LS06 hex open-collector inverter, uses bipolar transistor (“TTL”) gates with a supply voltage of 5 V and logic levels of 0 and 5 V.

The circuit between U1 and U2 uses a 2N7000 N-channel MOSFET to convert the 3.3V output of U1 to a 5 V input for U2:

- When the source is low, the gate-source voltage (V_{GS}) is 3.3 V, the transistor conducts and the drain terminal is pulled low.

- When source is high, V_{GS} is 0 V, the transistor is off and the drain terminal is pulled up to 5 V.

The interesting feature of this circuit is that pulling the drain terminal low pulls the source low through the “body diode”¹. This allows bidirectional logic level conversion between two open-collector outputs. For example, a sensor with a 5 V I2C interface and a microcontroller with 3.3 V IO.

The 74LS06 has open-collector outputs that can be pulled up to any voltage up to 30 V. The output can sink up to 40 mA, enough to drive small loads directly or as a driver for higher-power semiconductors. Since V_{IH} is 2 V it can be driven from a 3.3 V CMOS logic output. This IC can thus convert 3.3 V or 5 V logic levels to any other logic level.

Components

You will need the following from your ELEX 2117 parts kit:

- your CPLD board
- 74HC14 hex Schmitt trigger input inverter
- 74LS06 hex open-collector inverter
- 2N7000 n-channel MOSFET
- 4×1 kΩ resistors
- 100 nF capacitor
- your breadboard, some hookup wire and M-F jumpers
- a USB flash drive

You will need to use the lab ’scopes to make the measurements and a USB flash drive to save ’scope screen captures.

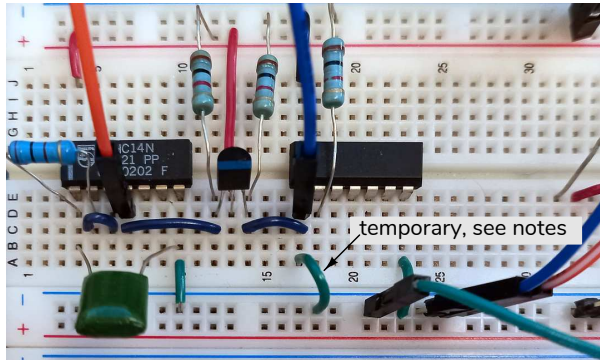
¹MOSFETs are actually 4-terminal devices. For an n-channel transistor the control voltage is applied between the gate and the P substrate. In most packages the P substrate is connected to the source. This results in a PN “body” diode from source to drain as shown above and in some MOSFET schematic symbols.

Procedure

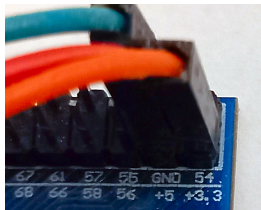
Test Circuit

Assemble the circuit shown above using components from your ELEX 1117 and 2117 parts kits. Consult the 74HC14 and 74LS06 datasheets on the course web site for pin-outs and specifications. Connect unused IC inputs to V_{CC} or ground.

The photo below shows an example of how the circuit could be built². Note the two supply rails (one for 5 V and one for 3.3 V).



Use the 5 V and 3.3 V supplies from the CPLD board (the ground, 3.3 V and 5 V pins are on the pin headers at the upper right of the board):

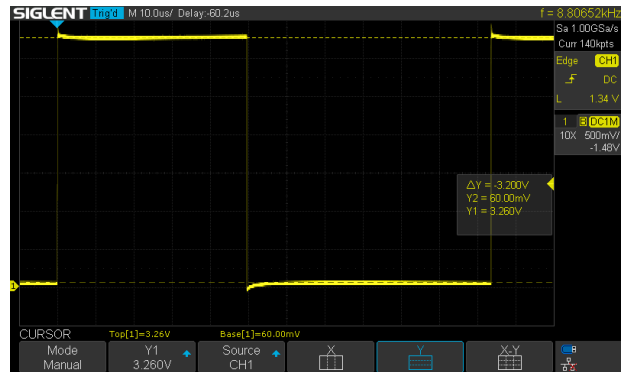


WARNING: Do not connect the 5 V and 3.3 V supplies together. This may destroy your CPLD.

The CPLD gets its 5 V supply from a USB port. Although the nominal USB supply voltage is $5\text{ V} \pm 5\%$, a device may see as little as 4.0 V under some conditions.

Connect the scope to test point 1 (TP1). You should see a square wave with levels of approximately 0 V and 3.3 V:

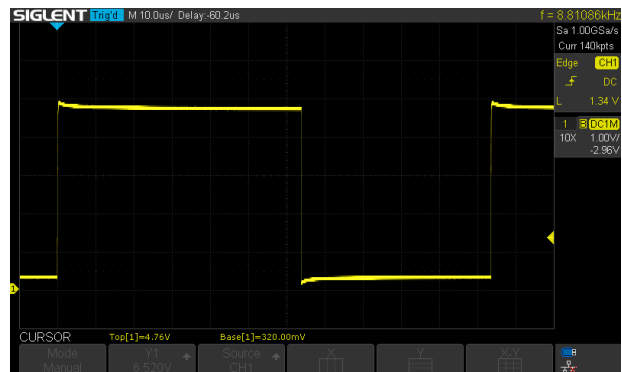
²Unused logic inputs should be tied high (for TTL) or low. However the U1 Schmitt trigger inputs and U2 TTL inputs are less sensitive to noise than CMOS logic inputs and may be left disconnected (floating) for this lab if desired.



Record a screen capture of the 'scope display for your report. The display should show the voltage scale. Make sure the levels displayed make sense before taking a screen capture. Plug your USB flash drive into the USB Flash Drive socket on the 'scope and use the 'scopes "Print" (or similar) feature to write the screen capture to your USB Flash drive. Do not use your phone camera to record the lab 'scope screen unless the lab instructor has approved this.

Connect the transistor's drain (TP2, U2 pin 1) to ground³, observe the effect on TP1 (U1 pin 4) and record your observations for your report.

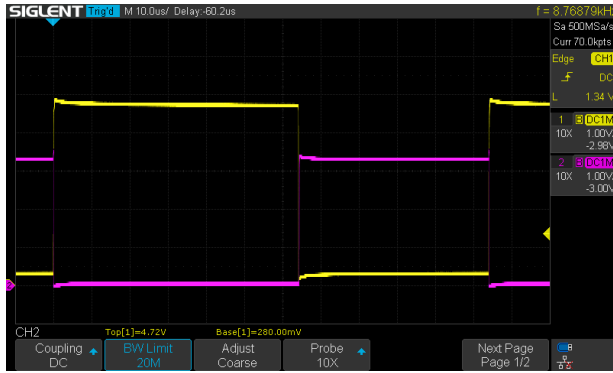
Remove the ground on TP2 and check the waveform on TP3. You should see a 5 V square wave:



Take a second screen capture for your report.

Connect probes to TP1 and TP3 simultaneously. You should see TP1 inverted and at 5V on TP3:

³Do this briefly; U2 does not have open-collector outputs but should tolerate its output being short-circuited briefly.



There's no universal wiring colour scheme, but some conventions are common. For DC circuits: red is the positive supply, black is common, and green is ground. Other colours may mean anything; often these are signals. Be consistent.

Cables with many wires, or wire pairs, often use colour, or colour pairs, to identify circuits rather than to give them meaning.

Take a third screen capture for your report.

Switch the pull-up resistor to 3.3 V and observe the effect on the output. Record your results and take fourth screen capture for your report.

Report

Show your working circuit to the instructor to get a mark for completing the lab.

Submit a report to the appropriate assignment folder that includes the following:

- Screen capture 1 of the signal at TP1 showing the two voltage levels.
- A description of what happens at TP1 when TP2 is grounded and a brief (1 sentence) explanation.
- Screen capture 2 of the signal at TP3 and brief explanation for the voltage level.
- Screen capture 3 of the waveforms at both TP1 and TP3 showing the voltage levels over one or two periods of the waveform and a description of how the two signals are related to each other.
- Screen capture 4 of the signal at TP3 with the pull-up connected to 3.3 V and a brief explanation for the change in logic level.
- A calculation of the power dissipated by R4 when TP3 is low and R4 is connected to (a) 3.3 V and (b) 5 V.

Appendix A - Wire Colour Conventions

Electrons have no fashion sense and so they don't care about the colours of the wires they travel on. However, anyone that needs to follow your wiring will appreciate it if you use a consistent wiring colour scheme, preferably one that they're familiar with.