Simulation

Introduction

In this lab you will design a circuit that detects if a signal is early or late relative a reference signal. Such circuits can be used to synchronize two devices so they operate at the same speed and in phase with each other. You will test your design by simulating it.

Requirements

In addition to `clk` (clock) and `reset` inputs, the circuit has two signal inputs: `xref`, and `x`, and two outputs: `early` and `late`. The outputs are set as follows:

- If `x` is asserted before `xref` then `early` should be asserted for one clock period after `x` is asserted.
- If `xref` is asserted before `x` then `late` should be asserted for one clock period after `xref` is asserted.
- If both `xref` and `x` are asserted at the same time then neither `early` nor `late` should be asserted.
- The falling edges of `x` and `xref` are ignored.

Each test vector should have five values: the input values of `reset`, `xref`, and `x`, and the expected output value of `early` and `late`. The first test vector should assert `reset`. Then your test vectors should apply inputs where: (1) `xref` and `x` are synchronized and the same duration, (2) `xref` and `x` are synchronized but different durations, (3) where `x` is asserted before `xref`, (4) where `xref` is asserted before `x`.

Procedure

Write a module that implements the synchronizer module described above and a testbench for it. You should be able to use the example in the lecture notes with some small changes. Remember to follow the course coding guidelines, including adding a comment at the beginning of the file with your name and the date.

Follow the procedure in Software Installation and Use document and the video on the course web site to create a simulation project, add the file(s) with your modules to the project and compile them. Add the `reset`, `clock`, `xref`, `x`, `early` and `late` signals to the Wave window. Run the simulation. The Transcript window should show any messages generated by the testbench and the Wave window should show the signal waveforms.

Report

Submit a PDF file to the appropriate Assignment folder that includes the following:

- (a) listing(s) of your testbench and DUT modules
- a screen capture of the simulation waveforms similar to that in Figure 1 or Figure 2.
- a screen capture of the Transcript window showing the messages generated by running the simulation. For example:

```
VSIM 5>run -all
# ** Note: $stop    : C:/Users/User/2117/lab6/lab6.sv(52)
#    Time: 17 us  Iteration: 2  Instance: /lab6_tb
# Break in Module lab6_tb at C:/Users/User/2117/lab6/lab6.sv line 52
```

Sample Test Vectors

You can write the following lines to a text file with a `.csv` file name extension to use as your test vectors:

```
1,0,0,0,0
0,0,0,0,0
0,1,1,0,0
0,1,1,0,0
0,0,0,0,0
0,1,1,0,0
0,1,1,0,0
0,1,0,0,0
0,0,0,0,0
0,0,1,1,0
0,1,1,0,0
0,1,0,0,0
0,0,0,0,0
0,1,0,0,1
0,1,1,0,0
0,0,1,0,0
0,0,0,0,0
```

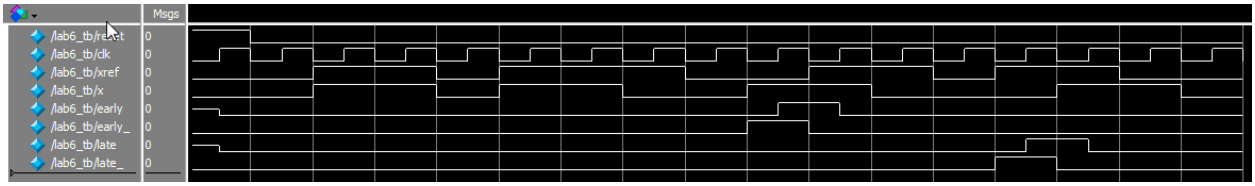

Figure 1: Simulation waveforms (Modelsim screen capture).

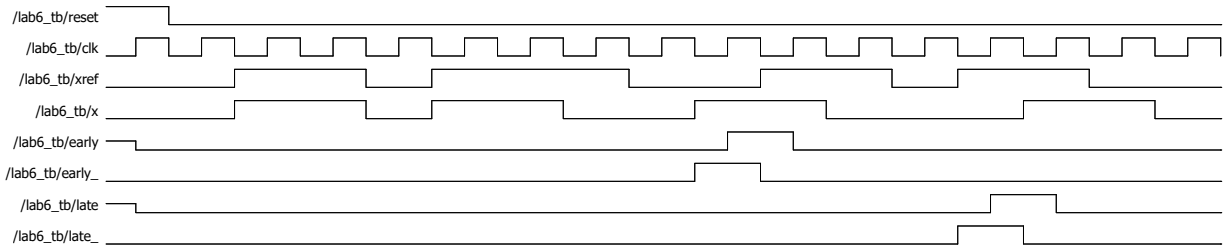

Figure 2: Simulation waveforms (Modelsim Print to PDF).