ELEX 2117 : Digital Techniques 2
2023 Winter Term

FINAL EXAM
14:30 – 17:30
Monday, April 17, 2023
SW03-1850

This exam has eleven (11) questions on four (4) pages. The marks for each question are as indicated. There are a total of thirty-eight (38) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

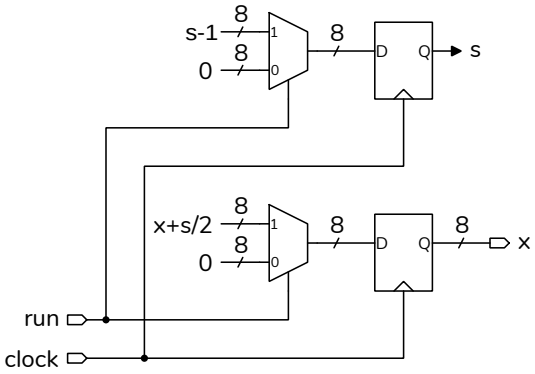
BCIT ID: _____

Signature: _____

0

Question 1 — 5 marks

Write a Verilog module named **`xpos`** corresponding to the diagram shown below. The module has a **`1`**-bit input **`run`**, a clock input **`clock`**, and an **`8`**-bit registered output **`x`**. Bits should be numbered in decreasing order. Follow the course coding conventions. You may omit comments.



Question 2 — 8 marks

Fill in the table below with the value of each expression. Give your answers as Verilog numeric literals including the length and using a hexadecimal base. Assume the following declarations:

```
logic [7:0] x = 8'hac ;
logic [3:0] y = 4'b1001 ;
```

expression	value
`{x[3:0],y[3:0],x[7:4]}`	
`!x && x`	
`~x | x`	
`x << 2 + 2'd3`	
`y/2`	
`x[3:0] > y`	
`x^y`	
`x[0] ? x : y`	

Question 3 — 3 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	truth value in an expression (0/1)	logic level (H/L)	Verilog value when input (0/1)
$\overline{\texttt{busy}}$	T	1	L	0
dark	F			
even*		0		
$\overline{\texttt{short}}$			L	

Question 4 — 4 marks

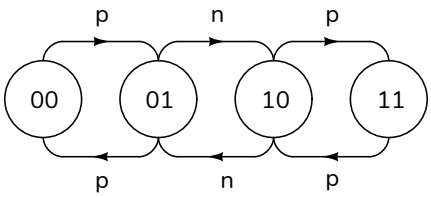
A module with inputs **p** and **n**, and a clock signal, **clock**, is declared as:

```
module statemachine
  ( input logic p, n, clock,
    output logic [1:0] state ) ;

   // your code here

endmodule
```

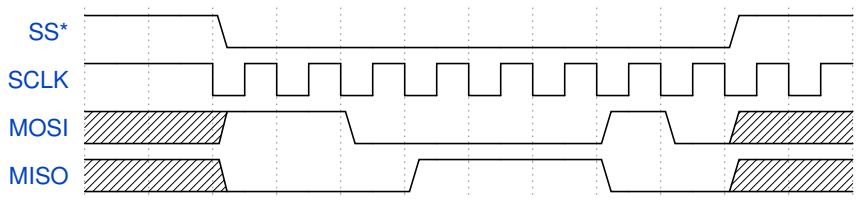
The module's behaviour can be described as a state machine with four states that have values **2'd0** through **2'd3**. The state transitions are as described in the state transition diagram below:



Write (a) Verilog statement(s) below that, if placed after the comment, would result in the behaviour described in the state transition diagram above. Do not repeat code already given. Follow the course coding conventions. You may omit comments.

Question 5 — 4 marks

The following waveform shows signals on an SPI interface that transfers bits most-significant-bit first. How many bits were transferred in each direction? What value was transmitted from the master to the slave? What value was transmitted from the slave to the master? Give you answers as a hexadecimal number. Show your work.



Question 6 — 2 marks

The maximum propagation delay through any combinational logic path in a CPLD is 17 ns, the minimum setup time of its registers is 2 ns and the maximum clock-to-output delay is 1 ns. What is the fastest clock frequency at which this CPLD can operate?

Question 7 — 2 marks

A digital power quality analyzer needs to measure the level of harmonics up to the 50'th harmonic of the 60 Hz power line frequency (i.e. up to 3000 Hz) with a quantization SNR of over 80 dB.

What minimum ADC sampling rate is required? What number of bits of resolution is required?

Question 8 — 2 marks

You are choosing the logic levels for a new design and need to maintain a noise margin of 1.5 V for both high and low logic levels. $V_{\mathrm{IL(max)}}$ is 2 V and $V_{\mathrm{IH\ (min)}}$ is 3 V. What are $V_{\mathrm{OL(max)}}$ and $V_{\mathrm{OH(min)}}$?

Question 9 — 2 marks

A CMOS digital logic circuit operates from a 1.5 V battery for 20 hours before the battery is exhausted. How long would the same battery last if the clock frequency was reduced by a factor of 20? *Hint: Battery life is inversely proportional to current consumption.*

Question 10 — 1 marks

Draw the schematic of a two-input NOR gate with an *open-drain* output. Use MOSFET transistors.

Question 11 — 5 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

fabless	
die	
TQFP	
wafer	
CPLD	

(1) manufacturer

(2) chip

(3) programmable

(4) package

(5) 300 mm

ELEX 2117 : Digital Techniques 2

2023 Winter Term

FINAL EXAM

14:30 – 17:30

Monday, April 17, 2023

SW03-1850

This exam has eleven (11) questions on four (4) pages. The marks for each question are as indicated. There are a total of thirty-eight (38) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

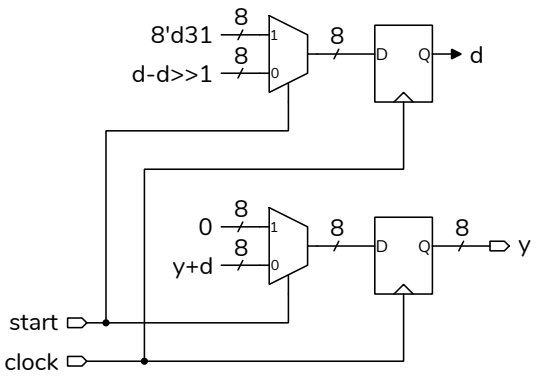
Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 5 marks

Write a Verilog module named **`vpos`** corresponding to the diagram shown below. The module has a **`1`**-bit input **`start`**, a clock input **`clock`**, and an **`8`**-bit registered output **`y`**. Bits should be numbered in decreasing order. Follow the course coding conventions. You may omit comments.



Question 2 — 8 marks

Fill in the table below with the value of each expression. Give your answers as Verilog numeric literals including the length and using a hexadecimal base. Assume the following declarations:

```
logic [7:0] x = 8'hca ;
logic [3:0] y = 4'b1001 ;
```

expression	value
`{x[3:0],y[3:0],x[7:4]}`	
`!x && x`	
`~x | x`	
`x << 2 + 2'd3`	
`y/2`	
`x[3:0] > y`	
`x^y`	
`x[0] ? x : y`	

Question 3 — 3 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	truth value in an expression (0/1)	logic level (H/L)	Verilog value when input (0/1)
$\overline{\texttt{busy}}$	T	1	L	0
dark	T			
even*		1		
$\overline{\texttt{short}}$			L	

Question 4 — 4 marks

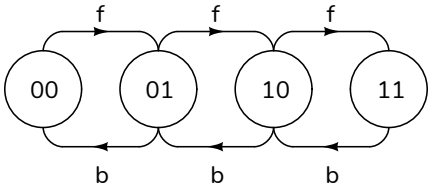
A module with inputs **f** and **b**, and a clock signal, **clock**, is declared as:

```
module statemachine
  ( input logic f, b, clock,
    output logic [1:0] state ) ;

   // your code here

endmodule
```

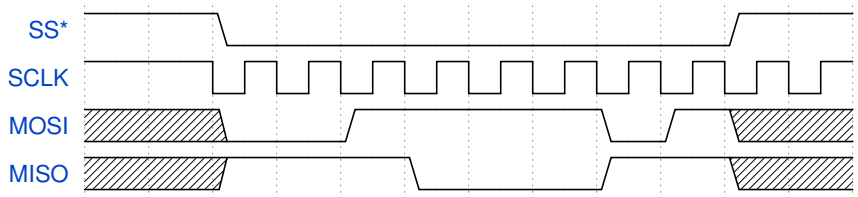
The module's behaviour can be described as a state machine with four states that have values **2'd0** through **2'd3**. The state transitions are as described in the state transition diagram below:



Write (a) Verilog statement(s) below that, if placed after the comment, would result in the behaviour described in the state transition diagram above. Do not repeat code already given. Follow the course coding conventions. You may omit comments.

Question 5 — 4 marks

The following waveform shows signals on an SPI interface that transfers bits most-significant-bit first. How many bits were transferred in each direction? What value was transmitted from the master to the slave? What value was transmitted from the slave to the master? Give you answers as a hexadecimal number. Show your work.



Question 6 — 2 marks

The maximum propagation delay through any combinational logic path in a CPLD is 7 ns, the minimum setup time of its registers is 2 ns and the maximum clock-to-output delay is 1 ns. What is the fastest clock frequency at which this CPLD can operate?

Question 7 — 2 marks

A digital power quality analyzer needs to measure the level of harmonics up to the 40'th harmonic of the 60 Hz power line frequency (i.e. up to 2400 Hz) with a quantization SNR of over 60 dB.

What minimum ADC sampling rate is required? What number of bits of resolution is required?

Question 8 — 2 marks

You are choosing the logic levels for a new design and need to maintain a noise margin of 1 V for both high and low logic levels. $V_{IL(max)}$ is 2 V and $V_{IH\ (min)}$ is 3 V. What are $V_{OL(max)}$ and $V_{OH(min)}$?

Question 9 — 2 marks

A CMOS digital logic circuit operates from a 1.5 V battery for 20 hours before the battery is exhausted. How long would the same battery last if the clock frequency was reduced by a factor of 10? *Hint: Battery life is inversely proportional to current consumption.*

Question 10 — 1 marks

Draw the schematic of a two-input NAND gate with an *open-drain* output. Use MOSFET transistors.

Question 11 — 5 marks

For each term in the left column write the number of the most appropriate match in the right column. There is only one best match for each term. No marks will be deducted for wrong answers.

fabless	
die	
TQFP	
wafer	
CPLD	

(1) 300 mm

(2) chip

(3) package

(4) manufacturer

(5) programmable