ELEX 2117 : Digital Techniques 2
2022 Winter Term

Quiz 3
13:30 – 14:00
Friday, April 1, 2022
SW03-1710

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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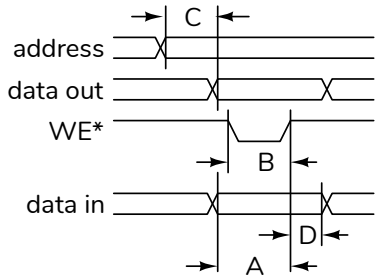
Question 1 — 4 marks

Write the letter from the following list: (A) byte-erasable, (B) fast, (C) non-volatile, (D) volatile, that best matches each of the following memory technologies. Use each letter once.

flash memory: C EEPROM: A cache: B SRAM: D

Question 2 — 4 marks



Write the appropriate letter from the timing diagram on the left for each of the following RAM timing specifications:

access time: C setup time: A

hold time: D pulse width: B

Question 3 — 4 marks

A circuit uses flip-flops with a required minimum setup time of 3 ns. The combinational logic in the circuit has paths with delays between 10 ns and 20 ns. The clock-to-output delay is 2 ns. At what maximum clock frequency will this circuit operate reliably? Show your work and include units.

$T_{su(avail)} = T_{clock} - T_{co} - T_{PD} = T_{su(min)}$ at max. f_{clock}

$T_{clock} = T_{su(min)} + T_{co} + T_{PD} = 3 + 2 + 20 = 25$ ns

$f_{clock} = \frac{1}{T_{clock}} = \frac{1}{25 \times 10^{-9}} =$ 40 MHz

Question 4 — 3 marks

You need to design a 32 kByte memory with a word size of 16 bits using 8k×4 ICs. (a) How many IC's will be needed in each memory bank? (b) How many memory banks will be needed? (c) How many address bus bits will connect directly to each IC?

(a) 16 bits/word ÷ 4 bits/IC = 4 ICs/word

(b) 32 kB/2 B/word ÷ 8k words/bank = 2 banks CORRECTED APR. 13

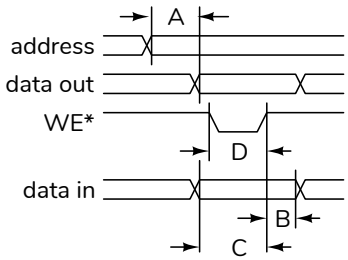
(c) $\log_2(8k) = \log_2(2^3 \cdot 2^{10}) =$ 13 bits

Question 1 — 4 marks

Write the letter from the following list: (A) byte-erasable, (B) fast, (C) non-volatile, (D) volatile, that best matches each of the following memory technologies. Use each letter once.

EEPROM: A cache: B SRAM: D flash memory: C

Question 2 — 4 marks



Write the appropriate letter from the timing diagram on the left for each of the following RAM timing specifications:

access time: A setup time: C

hold time: B pulse width: D

Question 3 — 4 marks

A circuit uses flip-flops with a required minimum setup time of 5 ns. The combinational logic in the circuit has paths with delays between 10 ns and 30 ns. The clock-to-output delay is 5 ns. At what maximum clock frequency will this circuit operate reliably? Show your work and include units.

$T_{su(avail)} = T_{clock} - T_{co} - T_{PD} = T_{su(min)}$ at max. f_{clock}

$T_{clock} = T_{su(min)} + T_{co} + T_{PD} = 5 + 5 + 30 = 40\ ns$

$f_{clock} = \frac{1}{T_{clock}} = \frac{1}{40 \times 10^{-9}} = 25\ MHz$

Question 4 — 3 marks

You need to design a 64 kByte memory with a word size of 32 bits using 8k×4 ICs. (a) How many IC's will be needed in each memory bank? (b) How many memory banks will be needed? (c) How many address bus bits will connect directly to each IC?

(a) 32 bits/word ÷ 4 bits/IC = 8 ICs/word

(b) 64 kB/4B/word ÷ 8k words/bank = 2 banks

CORRECTED APR. 13

(c) $\log_2(8k) = \log_2(2^3 \cdot 2^{10}) =$ 13 bits