

## Solutions to Quiz 2

### Question 1

There were different versions of this question with different bit widths, parameter names and default parameter values.

Write the declaration (the `module` statement) for a module named `smooth` that has: (1) a parameter named `n` (or `k`) with a default value of 8 (or 4), (2) a 16 (or 12)-bit logic input named `in`, (3) a 16 (or 12)-bit logic output named `out`, and (4) a logic input named `clock`. Do not write the body of the module or `endmodule`.

### Answer

```
module smooth
  #(parameter n=8)
  ( input logic [15:0] in,
    output logic [15:0] out,
    input logic clock );
```

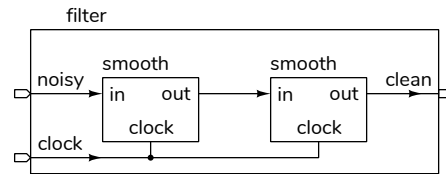
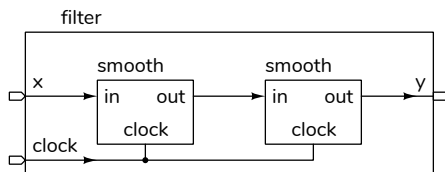
// alternate:

```
module smooth
  #(parameter k=4)
  ( input logic [11:0] in,
    output logic [11:0] out,
    input logic clock );
```

### Question 2

There were different versions of this question with different bit widths, parameter names and port names.

Write a module named `filter` that has a 16 (or 12)-bit input named `noisy` (or `x`), a 16 (or 12)-bit output named `clean` (or `y`) and a `clock` input. Instantiate two copies of the `smooth` module, connecting them as shown at right below. The value of the parameter `n` (or `k`) should be 4 for the `smooth` module left on and 8 for the one on the right. Declare any signals required to connect the modules. You may use any port-to-signal mapping style.



### Answer

```
module filter
  ( input logic [15:0] noisy,
    output logic [15:0] clean,
    input logic clock );

  logic [15:0] s ;

  smooth #(.n(4)) s0 (.in(noisy),.out(s),.clock );
  smooth #(.n(8)) s1 (.in(s),.out(clean),.clock );

  // also correct:
  // smooth #(4) s0 (noisy,s,clock) ;
  // smooth      s1 (s,clean,clock) ;

endmodule
```

### Question 3

Would a signal named `open` (or `closed`) have a high or a low logic level when a door is open (or closed)?

### Answer

- `open` is active-low; if the door is open then the truth value is true and the logic level should be low.
- `closed` is active-high; if the door is closed then the truth value is true and the logic level should be high.