# Quiz 2
**13:30 – 14:00**
**Friday, February 18, 2022**
**SW01-1021**

This exam paper is for:

## Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

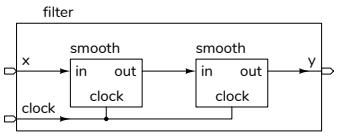
| Question | Mark | Max. |
|---|---|---|
| 1 | | 2 |
| 2 | | 6 |
| 3 | | 1 |
| Total | | 9 |

## Question 1 — 2 marks

Write the declaration (the **`module`** statement) for a module named **`smooth`** that has: (1) a parameter named **`k`** with a default value of 4, (2) a 12-bit logic input named **`in`**, (3) a 12-bit logic output named **`out`**, and (4) a logic input named **`clock`**. Do not write the body of the module or **`endmodule`**.

## Question 2 — 6 marks

Write a module named **`filter`** that has a 12-bit input named **`x`** a 12-bit output named **`y`** and a **`clock`** input. Instantiate two copies of the **`smooth`** module, connecting them as shown at right. The value of the parameter **`k`** should be 4 for the **`smooth`** module left on and 8 for the one on the right. Declare any signals required to connect the modules. You may use any port-to-signal mapping style.




## Question 3 — 1 marks

Would a signal named **`closed`** have a high or a low logic level when a door is closed?

255

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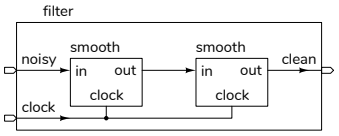
## Question 1 — 2 marks

Write the declaration (the **`module`** statement) for a module named **`smooth`** that has: (1) a parameter named **`n`** with a default value of 8, (2) a 16-bit logic input named **`in`**, (3) a 16-bit logic output named **`out`**, and (4) a logic input named **`clock`**. Do not write the body of the module or **`endmodule`**.

## Question 2 — 6 marks

Write a module named **`filter`** that has a 16-bit input named **`noisy`** a 16-bit output named **`clean`** and a **`clock`** input. Instantiate two copies of the **`smooth`** module, connecting them as shown at right. The value of the parameter **`n`** should be 4 for the **`smooth`** module left on and 8 for the one on the right. Declare any signals required to connect the modules. You may use any port-to-signal mapping style.




## Question 3 — 1 marks

Would a signal named $\overline{\texttt{open}}$ have a high or a low logic level when a door is open?