ELEX 2117 : Digital Techniques 2
2022 Winter Term

Quiz 1

13:30 – 14:00
Friday, January 21, 2022
SW01-1021

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: ______________________

BCIT ID: ______________________

Signature: ______________________

Question	Mark	Max.
Total		0

1. Write a Verilog module named **check** with two 7-bit inputs named **s1** and **s2** and a 1-bit output named **either**. **either** should be set to **1** if either **s1** or **s2** are non-zero. **either** should be set to zero otherwise. Declare arrays with decreasing bit order.

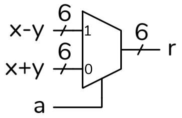
2. Given the following Verilog declarations:

```
logic [11:0] x = 12'd32 ;
logic  [7:0] y = 8'b101 ;
```

fill in in the table below with the value of the each expression as a hexadecimal (base 16) number (Verilog format not necessary) and the length (number of bits) as a decimal (base 10) number:

expression	value (in hexadecimal)	length (in bits, decimal)
{y,y}		
x[7:4]		
x && y		
x + y		

3. Write a Verilog statement that would implement the schematic on the right. You can assume it would replace the "missing statement" comment in the **quiz1** module.



```
module quiz1
   ( input logic [5:0] x, y,
     input logic a,
     output logic [5:0] r ) ;

   // missing statement

endmodule
```

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Name: ______________________________

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Question	Mark	Max.
Total		0

1. Write a Verilog module named **check** with two 15-bit inputs named **s1** and **s2** and a 1-bit output named **both**. **both** should be set to **1** if both **s1** and **s2** are non-zero. **both** should be set to zero otherwise. Declare arrays with decreasing bit order.

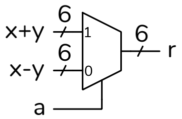
2. Given the following Verilog declarations:

```
logic [11:0] x = 12'd64 ;
logic  [7:0] y = 8'b111 ;
```

fill in in the table below with the value of the each expression as a hexadecimal (base 16) number (Verilog format not necessary) and the length (number of bits) as a decimal (base 10) number:

expression	value (in hexadecimal)	length (in bits, decimal)
{y,y}		
x[7:4]		
x && y		
x + y		

3. Write a Verilog statement that would implement the schematic on the right. You can assume it would replace the "missing statement" comment in the **quiz1** module.



```
module quiz1
   ( input logic [5:0] x, y,
     input logic a,
     output logic [5:0] r ) ;

   // missing statement

endmodule
```