ELEX 2117 : Digital Techniques 2
2022 Winter Term

MIDTERM EXAM 2
15:30 – 17:30
Friday, March 4, 2022
SW01-1205

This exam has five (5) questions on four (4) pages. The marks for each question are as indicated. There are a total of seventeen (17) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

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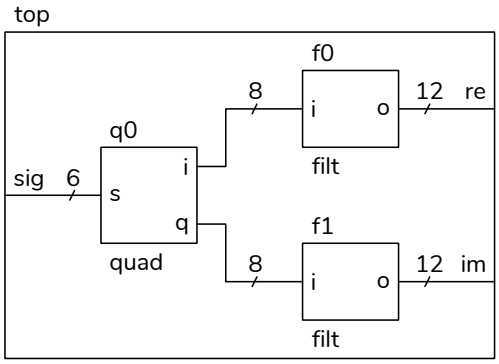
Question 1 — 7 marks

The following Verilog code shows the declaration of **quad** and **filt** modules. They diagram shows how they are connected within a **top** module:

```
module quad
  #(n=8)
   ( input  logic [n-1:0] s,
     output logic [  7:0] i, q ) ;
   // ...
endmodule

module filt
  #(m=12)
   ( input  logic [  7:0] i,
     output logic [m-1:0] o ) ;
   // ...
endmodule
```



The numbers above the signals show the signal (bus) widths. The identifiers above the boxes show the instance names. The identifiers below the boxes show the module names. The identifiers inside the boxes show the port names.

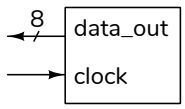
Write a System Verilog module named **top** that implements the diagram above. Declare any signals required to implement this module. Follow the course coding conventions.

Question 2 — 2 marks

Write System Verilog declaration for a two-dimensional array that models a lookup table of five rows, each containing a 6-bit value equal to the square of the row index. The array should be declared with row indices increasing from 0 to 4 and with decreasing bit indices. For example, the first value in the table would be 6'd0 and the last would be 6'b1000. You may use packed or unpacked arrays and any valid literal format.

Question 3 — 3 marks

The following diagram shows the signals making up an interface. The number of bits for each signal are shown above the signal, the arrow shows the port type (input or output) and the name of each signal describes its function.



Answer the following questions about this interface. Briefly (in one sentence or less) justify your answer.

- is it serial or parallel?

- is it synchronous or asynchronous?

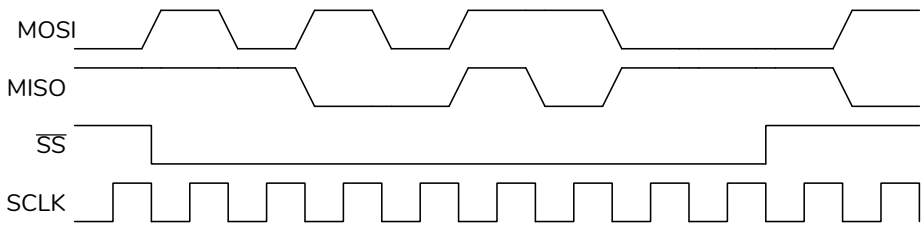
- is it uni-directional or bi-directional?

Question 4 — 3 marks

Fill in the blank boxes in the table below so that all values in each row are consistent (agree with each other). The first row is an example.

signal name	truth value (T/F)	logic level (H/L)	Verilog value as output (0/1)	Verilog value in expression (0/1)
$\overline{\text{hot}}$	T	L	0	1
alarm	T			
even*		L		
link			1	

Question 5 — 2 marks



The waveform above is measured on an SPI interface. What value was transferred from the slave to the master? Give your answer as a Verilog constant with the correct width and using a hexadecimal base. Show how you obtained your answer. Assume the bits are transferred most-significant-bit first.

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This exam paper is for:

Sample Exam 2 A01234567

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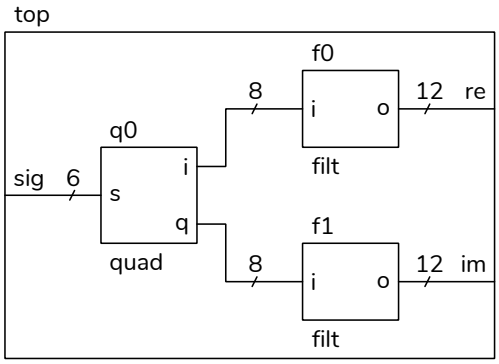

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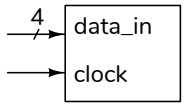

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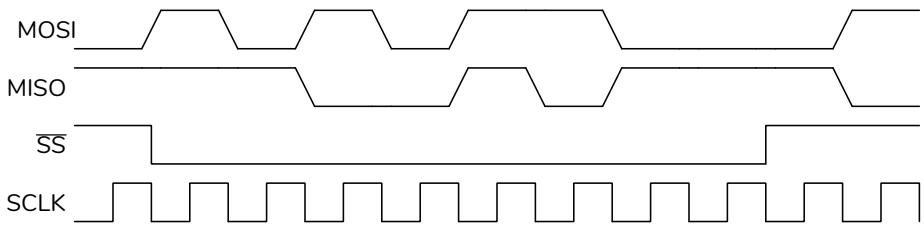

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