ELEX 2117 : Digital Techniques 2
2022 Winter Term

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MIDTERM EXAM 1
15:30 – 17:30
Friday, March 4, 2021
SW01-1205

This exam has three (3) questions on two (2) pages. The marks for each question are as indicated. There are a total of twenty-one (21) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		5
2		8
3		8
Total		21

Question 1 — 5 marks

A state machine has a one-bit **`reset`** input and a 3-bit **`value`** output. If **`reset`** is asserted the output is set to **`3'd1`**. When **`reset`** is not asserted the output takes on successive values of **`3'd4`**, **`3'd5`**, and **`3'd7`**. Then the output stays at **`3'd7`** until **`reset`** is asserted again. All changes on the output happen on the rising edge of the clock.

Write the state transition *table* for this state machine. Write the state and input values as Verilog literals in any base. You may also use `X` to indicate a "don't care" state or input value.

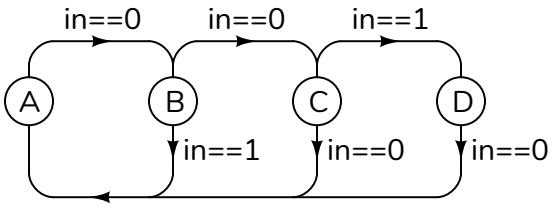
Question 2 — 8 marks

Draw the state transition diagram corresponding to the state transition table below. Label each state using the values shown below. **`in`** is an input declared **`input logic in ;`**. Label each transition with a Verilog expression that would have the value `1`. for that transition. You need not include transitions that would not change the state.

current state	input **`in`**	next state
0001	1	0010
0001	0	0001
0010	x	0100
0100	1	1000
0100	0	0100
1000	1	0001
1000	0	1000

Question 3 — 8 marks

Write a Verilog module named **`detector`** that implements the state state transition diagram shown below. It has a one-bit output **`out`**, a one-bit input **`in`**, and a clock input **`clk`**. **`out`** should be set to 1 only in state **`D`**. The output may change only on the rising edge of **`clk`**.



Follow the mandatory course coding conventions. Declare any signals (variables) required by your solution. You may use any state encoding. You may use any number of **`assign`** and **`always_ff`** statements. You may assume the initial state will be (A). *Hint: come up with a unique encoding for each of the four states.*

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0001	0	0001
0010	1	0100
0010	0	0010
0100	x	1000
1000	1	0001
1000	0	1000

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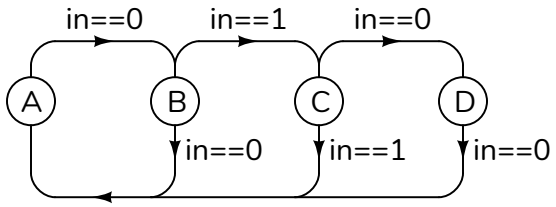

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