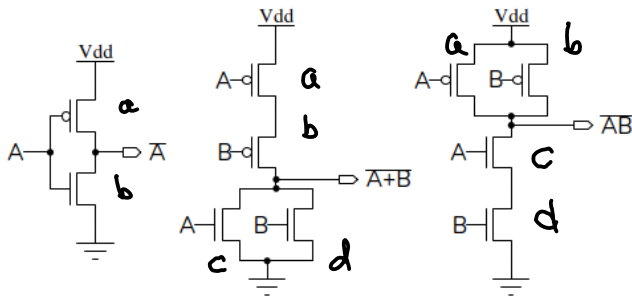# Implementation of Digital Logic Circuits

Exercise 1: Which transistors are on when the output is high? When it is low? In which direction does the output current flow in each case?

	NOT	NOR	NAND	current
low	b	c or d	c and d	in
high	a	a and b	a or b	out

Exercise 2: Which of these specifications does the manufacturer guarantee? Which are requirements?

V_{OH}, V_{OL} — guaranteed (outputs)

V_{IH}, V_{IL} — requirements (inputs)

Exercise 3: A logic family has $V_{OH}(min) = 5$ V, $V_{OL}(max) = 0.5$ V, $V_{IH}(min) = 4$ V and $V_{IL}(max) = 1.5$ V. What are the noise margins?

5V

0.5

4

1.5

$5 - 4 = \longrightarrow 1$ V

$1.5 - 0.5 \longrightarrow 1$ V

Exercise 4: All else being equal, by how much would we expect to decrease power consumption when reducing logic levels from 5 V to 3.3 V? What would be the effect on power consumption in reducing the clock frequency from 50 MHz to 1 MHz?

$$\frac{P_2}{P_1} = \left(\frac{3.3}{5}\right)^2 = 0.4 \quad \text{(reduced by 60\%)}$$

$$\frac{P_2}{P_1} = \left(\frac{1}{50}\right) = 0.02 \quad \text{(reduced by 98\%)}$$

Exercise 5: What are the active-state current and the RC time constant for a wired-or interrupt-request line using a 10kΩ resistor pulling up a circuit with 50 pF capacitance to 3.3 V?

$3.3\ V$

$10k$

$50pF$
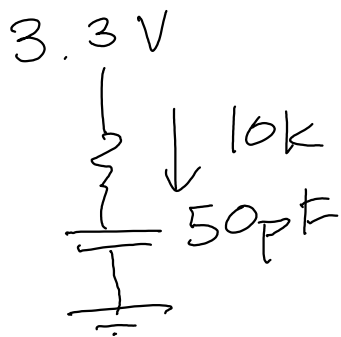
$$I = \frac{V}{R} = \frac{3.3}{10k} = 0.33\ mA$$
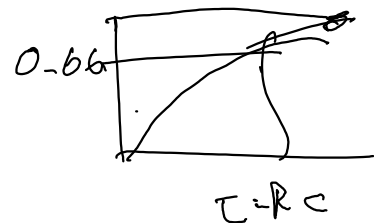
$$P = 1\ mW$$

$$V(t) = 3.3\left(1 - e^{-t/RC}\right)$$

$$C = RC = 10 \times 10^3 \cdot 50 \times 10^{-12}$$

$$= 560 \times 10^{-9}\ S.$$

$$= 0.5\ \mu s$$

0.66

$\tau = RC$

Exercise 6: How many square mm of PCB area does each package require? Which packages have their pins accessible when the packages is placed on the PCB?

$$22 \times 22 = 484\ mm^2 \quad \leftarrow \text{accessible pins}$$

$$3.5 \times 3.5 = 12.25\ mm^2 \quad \leftarrow \text{PCB pads covered by package}$$