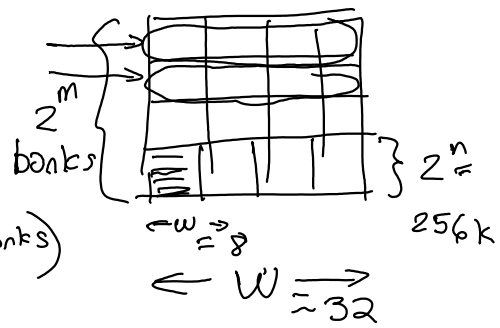
Memory System Design

Exercise 1: Is t_{AW} a requirement or a guaranteed specification for this memory? How about the t_{AA} ?

t_{AW} measured to $\overline{WE}$ (an input)
→ a requirement

t_{AA} measured to data out (on output)
→ a guaranteed response

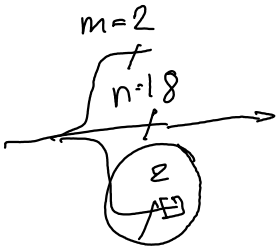
Exercise 2: How many 256 k×8 memory IC's would be required to build a 1 M ×32 memory? What is the width of the data bus? How many address bus bits would be required from the CPU? Which of these would connect to the memory ICs? What address values could be placed on the address bus? How many chip-select lines would be required?



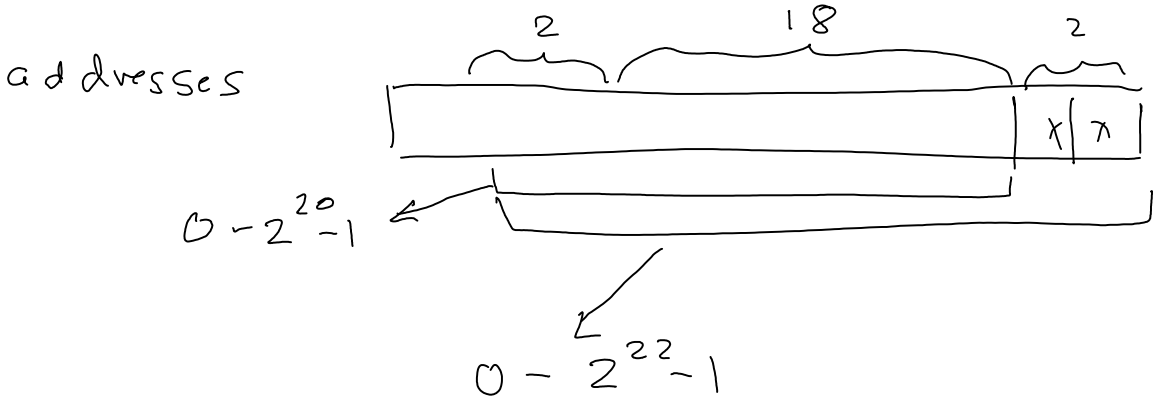
$2^m = 4 \quad \left(\frac{1M \text{ words}}{256k \text{ words/bank}} = 4 \text{ banks}\right)$

$2^n = 256k \quad n = 18$

$256k = 2^8 \cdot 2^{10} = 2^{18}$

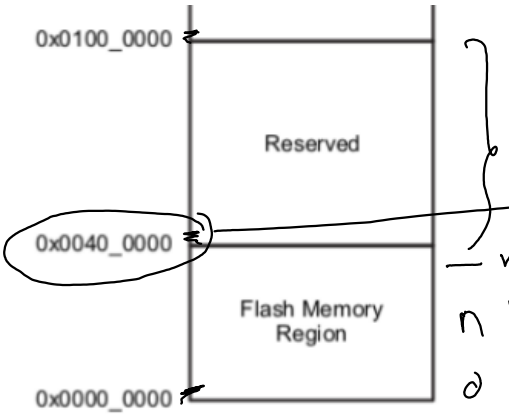


- need $4 \cdot 4 = 16$ ICs
- 32 bit data bus
- $18 + 2 = 20$ bits (n+m)
- n = 18 connect to the ICs



4 banks → 1 bank select per bank
∴ 4 bank select lines req'd.

Exercise 3: How large are the two lowest memory regions in the memory map above?



$0x\ 100\_0000$
$-\ 0x\ 40\_0000$
$= n\ 0x\ 0\_0000$ ← size

$n - 1$

n bytes → size is 0x40_0000

0

Exercise 4: If a CPU has a 32-bit address bus, how many bytes can it address? What range of addresses would correspond to the first 64 k Bytes? If this range of memory was to be implemented with 32-bit words, how many address bits would be required to select a byte within each word? How many bits would be required to select a 32-bit word within the 64 k range? How many bits are not directly connected to the memory ICs? What would they be used for?

32 bits → 2^{32} bytes $= 2^2 \cdot 2^{30} = 4$. 1 GByte

64k → 0 → 64k-1 : from 0 to 65535_{10}

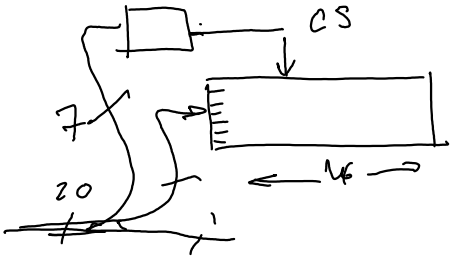
32 bit words need $\log_2\left(\frac{32}{8}\right) = \log_2(4) = 2$ bits

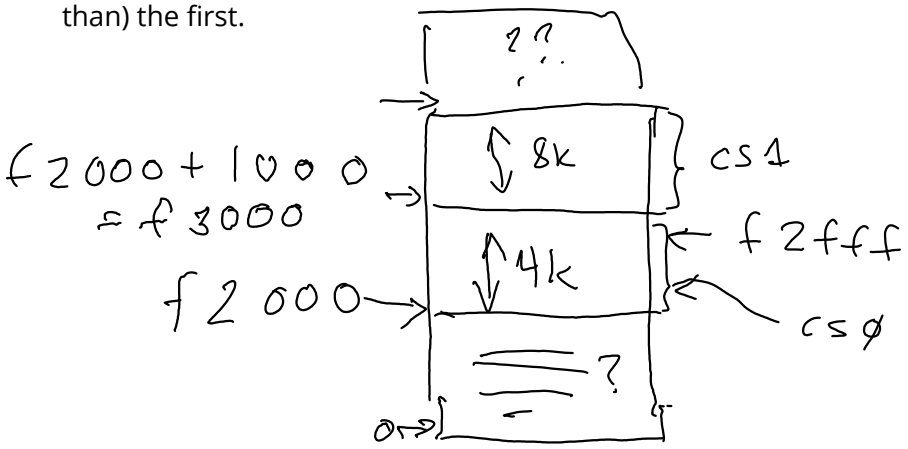
64k bytes $= \frac{64k \text{ bytes}}{4 \text{ bytes/word}} = 16k$ words.

$(n) = \log_2(16k) = 14$ bits

- 2 address bits (A_0 & A_1) not connected to ICs
- byte select within CPU.

Exercise 5: A 4k×16 memory is to be used in a system with a 20-bit address bus. This memory is to respond to addresses starting at 20'hf2000. Draw the memory map. Assuming the address signal is defined as `logic [19:0] a;` and the chip-select as `logic cs0 ;`, write the Verilog that would implement the chip-select signals csO. Write the expression for a second chip-select, `cs1` that would enable a second 8 kBytes bank immediately above (at a higher address than) the first.





1 byte select

$n = \log_2(4k)$

$= \log_2(2^2 \cdot 2^{10})$

$n = 12$

4k = 4096

0x1000

'h10000

```
assign
  cs0 = a >= 20'hf2000
        && a < 20'hf3000;
  [or   && a < (20'hf2000 + 4*1024);]

assign  cs1 = a >= 20'hf3000
        && a < (20'hf3000 + 20'h2000);
```